ON-BOARD SAR PROCESSING

R.W. Okkes
European Space Research & Technology Centre
Noordwijk, The Netherlands
G. Gaillat
Matra
Velizy, France
R. Schotter
Dornier Systems GmbH
Friedrichshafen, Germany
Comission II

ABSTRACT

This paper describes candidate concepts for on-board SAR processing covering the associated aspects of applicable algorithms, processing system architectures and technology.
Emphasis is placed on SAR image generation being the most demanding SAR pre-processing task.

1. INTRODUCTION

The processing of SAR data on-board of the spacecraft may serve two objectives:

a) enhancement of mission capabilities, and
b) improvement of facilities for data usage.

Enhancement of mission capabilities is achieved because on-board SAR imagery generation and coding provides for data volume reduction as compared to the amount of raw data generated by the sensor, which alleviates data transmission, data handling and on-board recording constraints.
The utilisation of sensor data may be improved because of the inherent capability of on-board processors to provide desired data products in real time being delivered to local relatively simple ground receiving stations for further processing or direct usage.

The type of processing envisaged can be characterised by its typical end-product i.e.:

a) SAR image generation
b) SAR image encoding
c) Data extraction (user oriented processing)

The image generation step can be considered as a necessary one for all follow-on processing and is therefore commonly identified as a "pre-processing" step.
The main processing parameters are related to the multi-look detection operation, providing a trade-off between image spatial resolution and the amount of "speckle", the latter disturbing component being introduced by the coherent microwave signal sensing mechanism. Apart from the selection of the multi-look operation the image generation step is essentially not effected by the user, which may consider its output as being generated by a microwave imaging sensor with predefined system characteristics.

Encoding of SAR imagery data (mono- or multi "spectral" data) is an operation aimed at removing redundant SAR imagery data end speckle distortion. Data reduction is achieved by entropy coding and image enhancement by adaptive speckle filtering. Because the processing is information preserving, it is as such transparent to the user.

Data extraction from imagery data is aimed at providing the user with specific types of information which is oriented towards a specific application, e.g. the extraction of sea-wave spectral data for oceanographic research purposes. Data extraction processing may result in a large reduction of data volume.

The image generation processing puts the most stringent requirements on the performance of the processing system and is therefore analysed further in this paper.

2. SAR IMAGE GENERATION PROCESSING

Table 1 gives the specification of a typical C-band radar sensor and in Table 2 the associated image specification for which the processing task will be analysed. The processing functions to be executed for image formation are (in segmential order): range compression, range migration correction, azimuth processing (specified later).
In addition to the main processing operations, data analysis is performed in order to feed the processor with updated mean Doppler and Doppler rate information, which varies with the satellite's orbital position.
Figure 1 depicts the block diagram of the overall processing system.

The selection of processing device technology is mainly governed by power and weight constraints. For range compression analog (Surface Acoustic Wave) devices outperforms digital device technology with this respect and is therefore applied prior to baseband convertion and ADC. Sample interpolation, associated with linear range migration correction is conveniently implemented by controlling the ADC sample instants. All remaining processing functions. i.e. those relevant to time stretching of the range samples arriving in bursts and azimuth processing are performed by a digital processing system.

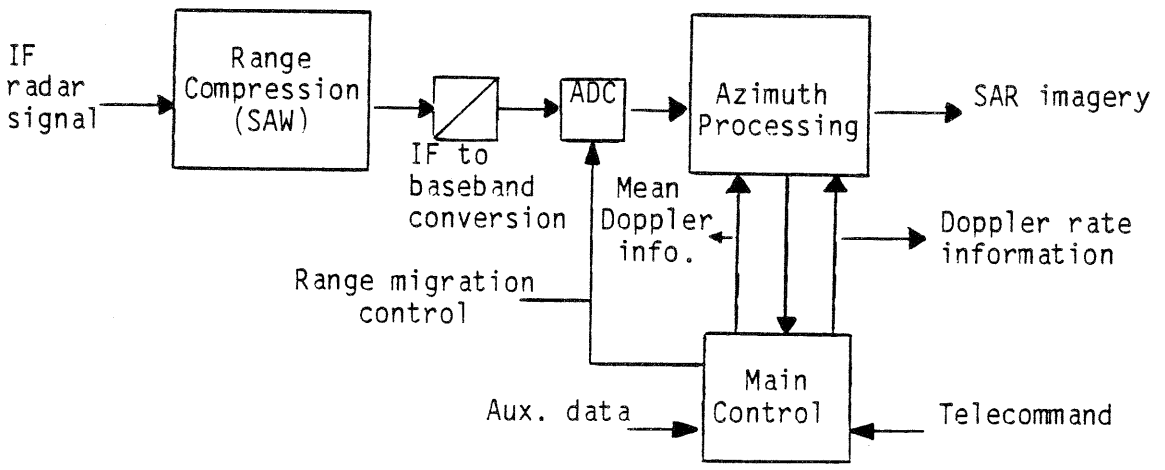

Fig. 1 - On-board SAR processing system diagram

Wavelength (C-band)	0.057m
Pulse repetition frequency	1690 Hz
Range sampling rate	16 MHz
Altitude	793 Km
Near incidence angle	18.4°
Far incidence angle	25.5°

Table 1 - Radar sensor specification

No. of range cells after compression	4800
Azimuth replica length	256
Azimuth resolution	25m
Ground range resolution	25m
Swathwidth	80-100 Km
Radiometric resolution	1.5 dB
No. of looks	4
Dynamic range of processor output signal	60 dB
Highest sidelobe level	-20 dB
Processor induced artifacts	-30 dB
Radiometric distortions	$\pm$ 0.5 dB
Output data registration errors	$\pm$ 1 pixel

Table 2 - Image specification for a typical earth exploration SAR-system.

It has been demonstrated that the most efficient azimuth compression algorithm for multi-look processing in terms of memory and arithmetic requirements is based on the "spectral analysis" or SPECAN methods (6). For this reason it is considered here merely for the purpose of dimensioning the azimuth processor.
The main azimuth processing characteristics relevant to the image specification given in table 2 are:

- Input data rate (burst mode) 38.4 Mbyte/s
- Number of FFT's of length 256/sec. 42250
- Output data rate 1.5 M pixel/s (8 bit)

Two different implementations for achieving the azimuth processing task, are outlined below.

2.1 Azimuth processing using the High Speed Programmable Processor (HSPP)

The High Speed Programmable Processor (HSPP) concept is developed by Matra and Saab under ESTEC contract and is intended to provide a unified tool for various kinds of high speed on-board signal processing. Real time optical or SAR imagery are typical applications. Implementation of an on-board image processing application have been discussed in (1). Processor architecture is described in (2) and (3).
In summary, HSPP is a bus oriented MIMD parallel processor allowing cooperation of various kind of processors such as general purpose microprocessors, digital original processors, specialised signal processing devices (e.g. FFT), etc. (see Fig. 1).

Communication between processors and with memories are performed through a double ring bus. It has been shown in (2) and (3) that with the selected protocol the double ring bus provides a high throughput (20 Mbytes/s) on a restricted number of wires (96) and can in fact be used as a conventional 3 state bus. Furthermore, the bus protocol ensures no waste of bus traffic, so that effective throughput can be equal to nominal throughput.

Two kinds of ring bus interface modules are provided to the processor or memory modules (abonnees), (a) the active bus interface (ABI) allowing an abonnee to send, read or write orders through the bus, and (b) the passive bus interface (PBI) allowing an abonnee to receive and respond to read and write orders from the bus.

Typically processor abonnees are interfaced through ABI's and memory abonnees through PBI's. Nevertheless, in some applications, including the present one, it may be interesting to interface processors through PBI's or through both ABI's and PBI's.

Both ABI and PBI contain a RAM simulating a double port access. One part is for processor accesses, the other for ring bus access. Data as well as exchange orders are contained in these RAM's. In fact, ABI or PBI merely appears as RAM locations on a bus internal to the abonnee. The rings bus function consists in routing data from one ABI RAM to a PBI RAM or viceversa according to an exchange order located in the requesting ABI RAM.

Two kinds of original processing abonness have been developed up to now. One is made out of an AMD 29116 processor associated with a 16x16 multiplier-accumulator. The other one is a cluster of up to 8 monochip Texas TMS 320 processors sharing access to ABI or PBI. In the present application, the second solution provides more processing power for a smaller power consumption.

2.1.1 SAR Processing implementation

From an implementation point of view, SAR image can be divided into the four following steps:

1. Input data samples are entered into a Main Corner Turning Memory (MCTM) range after range line in bursts.
2. Corner turned data is azimuth processed and consists per azimuth line of, reference function 256 point (complex) vector multiplication (including window weighting), 256 point FFT, square modulus detection and cummulative summation of selected output samples (look summation).
3. Look summed data is then entered into a Re-Corner Turning Memory (RCTM).
4. Each range line of RCTM is then deskewed and output.

Untill the deskew operation, each azimuth processing task is confined to a single range bin and hence, a straightforward inplementation consists in dividing the azimuth processing task over as many processors as necessary, each processor being in charge of a fraction of the total of 4500 azimuth processing looks. Typically, one TMS-320 processor needs 3.7 ms to perform 256 complex multiplications, a 256 point FFT, 256 (or less) square modulus computations and 256 (or less) accumulations of the results into a 256 word array containing the cumulative sum of 4 successive tools.

Since 42250 of such tasks are to be performed every second, 160 processors are needed to achieve the task. These 160 processors are divided into 20 clusters of 8 processors.

Similarly, deskewing one range is independent from deskewing another range, so that the task can be shared among several processors. About 4 µs are necessary for a TMS-320 to perform the cubic interpolation needed to compute each output point. Hence, since output rate is 1.5 Megapixels per second, 6 processors are needed for deskewing.

MCTM must contain at least 256 rows of 4800 points, i.e. 1.2 mega complex words. Since a complex word needs 2 bytes, 2.4 Megabytes are necessary. In fact, the easiest solution consists in providing three such banks, i.e. 7.2 Megabytes to allow "overlap" of azimuth processing tasks (5). In the same way, RCTM must contain 256 rows of 4800 points. Here, 8 bits real numbers are sufficient so that its size is 1.2 Megabyte. But here a flip flop mechanism is necessary: While azimuth processors perform look summations on one bank, the deskew processors read data from the other bank. Hence the RCTM size is 2.4 Megabytes.

In the proposed implementation (see Fig. 2), each of the 20 clusters of 8 azimuth processors is linked to the double ring bus through a PBI module. Each PBI module has a 480 K bytes Rams, 360 for MTCM ad 120 K for RCTM. Hence both MCTM and RCTM are divided among the 20 algorithm processing abonnees. The input data flow from the ADC is entered into HSPP via ABI's and routed towards MCTM through the double ring bus. 8 ABI's are necessary to handle the 38.4 MB/s input data flow. The rate on the bus is 16.2 MB/s (time stretched).

The 6 deskew processors are linked to double ring datas through one ABI module which reads datas from RCTM. Output data is then directly sent to the output coupler through the internal bus of the deskew processor.

They do not use ring busses. Input ABI's need small Rams (FIFO) for time stretching of the input data bursts and to allow some slight traffic fluctuations due to the bus mechanism. Deskew processors ABI needs a 64 Kbyte memory: two 4800 byte buffers used in a flip flop mode for each of the 6 deskew processors.

The azimuth processors needs for every set of 240 FFT's a new set of auxilliary data (reference function vector and information for output sample selection), which is generated by an external control unit. Multiplexing of auxilliary information with input data is performed through a dedicated ABI and input coupler.

The auxilliary data for the deskew processor is generated by the azimuth processors and sent along with the data block.

For the computation of mean Doppler information a selection of input data has to be made as follows:
- selection of one azimuth line out of 8
- selection of 64 consecutive range lines out of 256 (i.e. there are gaps of 192 range lines).

This is be done by connecting the mean Doppler processor via a PBI to the bus, which is loaded under control of the input ABI's. The PBI contains a corner turn memory of 80 kByte. The output of the mean Doppler processor is directly (i.e. not via ring bus) coupled to the external control unit.

It must be pointed out that the distributed implementation of MCTM and RCTM is possible thanks to the HSPP ring bus protocol. As explained in (2), each ring bus slot is statistically allocated to a group of memory chips. Such a protocol realisation has the property of high rate sequential, random or deterministic data communication via time multiplexed subflows thus avoiding memory access collision at chip level. Hence medium speed low power consumption Cmos random access memories can be used.

Synchronisation of the entire process is performed in a very simple way. Every time a set of lines is entered by input ABI's into MCTM, a flag is set in each PBI by input ABI's. When this flag is set, azimuth processors can begin processing the corresponding data and reset the flag. Since the input instrument has a fixed rate, input ABI's are not supposed to test the flag. Azimuth processors must have finished their job in time. Similarly, every time a block of data is ready in RCTM, Azimuth processor sets a flag to one in its PBI. When deskew processors have finished a set of tasks, they test this flag looking for another set of tasks. Doing this, they create a negligible extra traffic on the ring busses.

The total ring bus throughput is about 18 MB/s: 16.7 from input ABI's to MCTM and mean Doppler processor plus 1.5 from RCTM to deskew processors ABI. Such a throughput is compatible with the 20 MB/s system performance, essentially because the chosen ring bus protocol ensures no waste on bus traffic (see 1.). For higher throughputs, multiple bus HSPP coninuations such as those described in 2 would have been needed. Total throughput on all local busses is about 50 MB/s but does not constitute a bottleneck since it is divided over 28 abonnee local busses.

For the purpose of protecting the processing system against failures, spare modules should be added.

A main advantage of HSPP system as described in 3 is that ring buses are software reconfigurable with no loss in performance in case one abonnee fails. Hence a reliable architecture where all functions are provided with a spare module includes 11 input ABI's instead of the minimum of nine necessary, 23 PBI's and 21 clusters of 8 azimuth processors instead of 20, 2 deskew ABI's and 2 clusters of 6 deskew processors instead of one.

Mass and power consumption estimations of the entire processing system are indicated in table 3 for which semi custom implementations of ABI and PBI modules have been assumed. 8 K x 8 bit Cmos static rams have been considered. Due to low frequency accesses to these memories, their power consumption is close to their standly power consumption (0.5 mW). Only switched on processors have been taken into account for estimation of power consumption. Nevertheless a large part (70%) of system power consumption is due to digital signal processors. Two remarks can be made concerning this point: Firstly, the presently available N-mos Texas TMS-320 have been assumed. In fact, a Cmos version of TMS-320 has been announced which runs at one instruction every 120 ns instead of one instruction every 200 ns. Hence, even if chip power consumption is not reduced, total system power consumption will be reduced with about 40% since 96 azimuth processors will be needed instead of 160. The second observation is that TMS-320 have been assumed for every type of computations, including FFT's. Compared to presently available alternatives, they are quite attractive even for FFT's and have the advantage of being standard HSPP components. However, it is likely that in a near future efficient FFT chips like the one described in (4) will be

available. Since such a chip is 6 times as fast as TMS-320 for FFT computations a combination of 2 TMS-320's plus one FFT chip would favourably replace a cluster of 8 TMS-320's resulting in a 60% power reduction per processor cluster and a total of 100W for the azimuth processor.

2.2 Flexible Hardware Approach of a Synthetic Aperture Radar Processor and its Technological Aspects

A modular, realtime SAR-Processor Breadboard, based on the ESTEC SPECAN concept, is presently being developed by DORNIER under contract of DFVLR and funded by the German Ministry of Research and Technology (BMFT) (5). The digital ground processor resulting from these activities shall be able to produce two-dimensional SAR images taking raw radar data of the German X-band radar system MRSE (Microwave Remote Sensing Experiment) as well as the C-band ESA-ERS 1 system. Additionally, further adaptability of the processor to spaceborne/airborne SAR-systems shall be possible.

The basic features of the processor are given by the image specification listed in Table 2 which are regarded to be a common baseline for earth exploration purposes within ESA (European Space Agency) and DFVLR (German Authority for Aerospace Research). Furthermore, the processor concept is strongly influenced by a high throughput demand (realtime processing) at low power consumption rates in order to allow for a future upgrading of the processor to spaceborne/airborne applications.

Finally, a high modularity and, if possible, repeatability of functional groups within the processor is required for reasons of cost reduction and simple maintainability.

2.2.1 Processor Architecture

The architecture of the SAR-Processor Breadboard is shown in Fig. 2-1. It consists of a high speed radar data processing pipeline including the hardware modules.

- Reference Function
- Corner Turn Memory (CTM)
- Fourier Transformation (FFT)
- Look Summation (LS)
- Radiometric Correction (RC)
- Azimuth Deskew (AZD)
- Recorner Turn Memory (RCTM)
- Deskew (DSK)

which performs the azimuth compression, look summation and post-processing of 1024 range samples (appr. 20 km swathwidth) at an input data rate of up to 3 MHz. Identical hardware pipelines are paralleled if a full swath must be processed in realtime. In this case, two additional models

- Subswath formation (at the input)
- Full Swath formation (at the output)

are required for a complete processor (see Fig. 2-2).

Each fast processing pipeline is controlled by three medium speed control modules whic provide for the parameters required by the pipeline modules. At this control level control data must be computed at a rate of typically

2-10 K words/sec depending on the module and the SAR-sensor itself. Finally, a slow speed P-Controller forms the processor interface to the external environment.

Range compression and Linear Range Migration Correction are performed in front of the Azimuth Processor in a SAW device and by proper sampling control of the AD-converter (see Fig. 2-2), respectively.

2.2.3 Implementation of the processor

The implementation of the processor is accomplished under the aspect that each specifically designed hardware module must include enough commonality and flexibility to make it a part of a more general signal processing hardware family. This concept allows the functional modules to be used at several places of the processor (e.g. see Storage Unit) or even supports the implementation of different image processing tasks (e.g. other SAR-algorithms, pattern recognition etc.) at low development cost using the same hardware modules in different arrangements. Fig. 3-1 shows a block diagram of the signal processing hardware family.

Some of the more important modules of the SAR-Processor Breadboard are described in more detail in the subsections below.

2.2.3.1 High Speed Storage Unit

Intermediate storage of the data frames is one of the most important functions of any kind of image processing. In a SAR-processor those memory units are used during Corner Turning, Look Summation, Recorner Turning, video display storage and test pattern generation. In order to cover these applications a universal memory board has been developed which allows for writing and reading line based image data in both range and azimuth direction. The length of each line can be programmed within the total capacity of 256 Kwords, where the word length can be any value up to 16 bits.

The memory boards can easily be cascaded if more than 256 Kwords of memory size is required.

Dynamic NMOS memory chips (64 k 1) and TTL-ALS control circuits are used for the board, the size of which is 233x160 mm^2. A write/read speed of up to 3 Mwords/sec could be achieved at a power consumption of 3.2 Watt. Refresh circuits for the dynamic memory chips are included on the board.

A complete memory system (e.g. CTM) is built up of 3 memory boards and a simple controller board which provides for the correct input/output interface some trigger signals which tell the memory boards to write/read frames. The total power consumption of the CTM has been measured to be 13.5 Watt.

2.2.3.2 Finite Impulse Response Filter

FIR filters are widely used for low pass filtering, bandpass filtring (in combination with a complex premultiplication), digital interpolation and correlation. In a SAR-processor, digital interpolation/resampling is required for the postprocessing module.

A two-channel FIR filter offering programmable length of up to 256 samples at a word length of 16 bit (data and coefficients each) has been developed using a TRW multiplier/accumulator circuit and TLL-ALS control logic on a standard 233x160 mm^2 board. Subsampling of the output signal is possible if the FIR filter is used as a lowpass filter.

The maximum input data rate is given by the internal 12 MHz computation clock, the filter length and the chosen subsampling factor. At a filter length of 16 (no subsampling), the input rate can be up to 0.72 Mwords/sec. The power consumption is 9.1 Watt.

The filter coefficients are stored in a 2Kx8 PROM offering a large variety of different, selectable coefficient sets.

2.2.3.3 Complex Multiplication

A complex multiplication module has been developed on the basis of a fast TRW multiplier and some TTL-ALS control logic. The whole circuit is implemented on a board of the size 160x100 mm . It can operate up to an input data rate of 3 Mwords/sec. The power consumption turned out to be 3.0 Watt including output rounding and saturation limitation circuits. Data word length can be up to 16 bit at both input and output.

This unit is used as the Reference Function Multiplication module of the SAR-Processor. Additionally, detection and radiometric correction can be performed with minor changes of the hardware.

2.2.3.4 Fast Fourier Transformation (FFT)

A hardware FFT module is presently under design at DORNIER. It is based on the Radix 2 Decimation-in-Time algorithm showing the following features:

- complex input up to 16I, 16Q
- complex output up to 16I, 16Q
- Programmable FFT length of 32-64-128-256-512-1024-2048-4096
- complex butterfly hardware element, operating at approx. 15 MHz
- FFT data addressing scheme downloaded from external device.

This module will be able to perform the operations required for azimuth/ range compression of the SPECAN method as well as of the frequency domain algorithm.

2.2.3.5 Medium Speed Pipeline Controllers

The pipeline controllers of the SAR-Processor Breadboard convert the more general control parameters (e.g. Mean Doppler Frequency, FM-Rate, Antenna pointing angles) into secondary control parameters which are used by the pipeline modules. The basic arithmic operations are required in order to perform these transformations. Since the output data rates are around 2-10 Kwords/sec, a signal processor like the NEC 7720 is a favorite candidate for these jobs.

The EPROM version NEC 77P20 allows for a flexible programming of both the instructions ROM and data ROM.

2.2.4 Adaptation to on-board processing

On-board applications of the flexible hardware concept are characterized by stronger requirements with respect to

- electrical power consumption
- weight and volume
- reliability

For the Breadboard described the power consumption of a complete subswath processing pipeline (1024 range samples) including the pipeline controllers amounts to 85 Watt approximately. These circuits are located on 17 boards each of the size 233x160 mm at a height of 14 mm. Therefore, the active volume of the boards equals 8.8 liter at a total weight of 6 kg.

For an on-board SAR processor both power consumption and weight/volume could be reduced by

- use of high speed CMOS circuits
- use of chip carrier packages (i.s.o. IC sockets as for the Breadboard
- custom designed circuits for repetitive elements within the processor
- smaller connectors
- compressed layout of boards

Taking a pessimistic estimate of the improvements caused by the above measures a reduction by a factor of two for both power consumption and weight should be achievable.

Thus, typical figures for each on-board subswath processor would be:

power consumption = 40 Watt
weight (incl. frame) = 3.5 kg

The number of pipelines necessary for a full swath processor will be in the order of five. Additionally, more pipelines might be required due to reliability reasons. No reliability computations have been performed up to now for the on-board version of the processor.

The above budget of weight/volume and power consumption is not complete. Contributions of the Mean Doppler Tracker, FM-Tracker and the interface circuits to telemetry must be added.

CONCLUSION

The two different processing implementations analysed show that with to-day's technology an azimuth processor can be constructed consuming about 200W and weighting 20 to 25 kg. From the description of the architectures presented it is concluded that:

- The HSPP Concept uses standard bus interfaces and a standard bus protocol, which allows to implement at relative low cost multiprocessor architectures for a specific signal processing task. The processor performance is kept up to date by incorporating the latest available VLSI processing chips (DSP's or FFT chips). For example when the announced C-MOS versions of the TMS-320 DSP are used

for the azimuth processing application, the power consumption will be reduced to about 100W.

- The flexible hardware concept uses task dedicated standard modules belonging to a signal processing hardware family. Task dedication permits to save hardware as compared to more general purpose programmable DSP's and therefore potentially this approach leads to minimum power and weight architectures in combination with (semi) -custom VLSI technology.

However the relatively high cost related to VLSI (semi)-custom design and the construction and testing of task dedicated multi module parallel pipeline architectures and their control hardware may be prohibitive in exploiting fully its potential saving.

Hence each of the described architectures has its own (time evolving) specific merits which will determine the selection of its use for a specific application.

ACKNOWLEDGMENT

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FIGURE 1.1 - TYPICAL HSPP CONFIGURATION

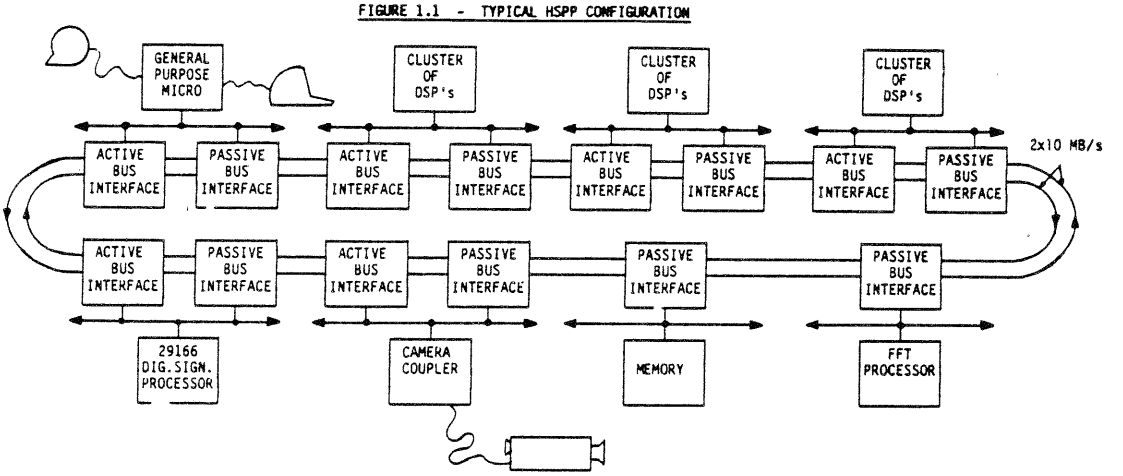
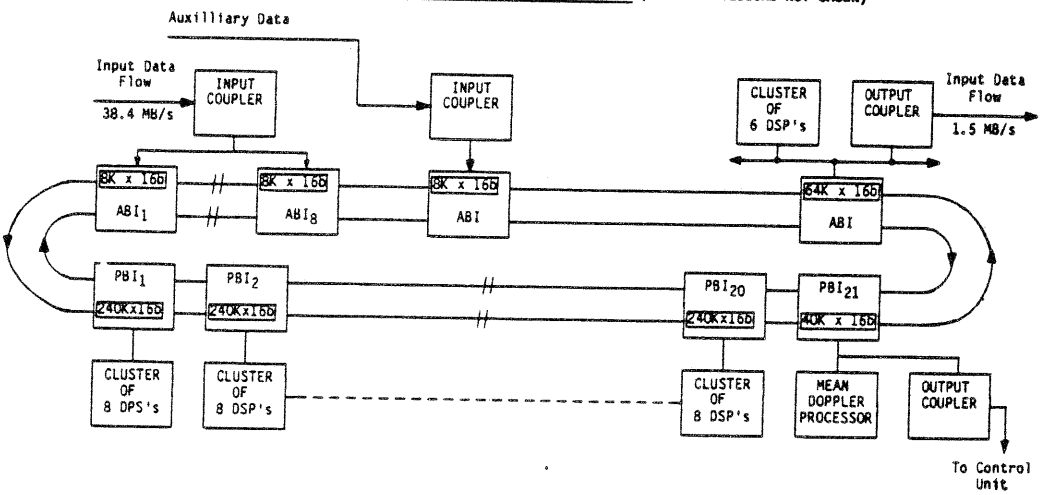


FIGURE 1.2 - HSPP IMPLEMENTATION OF SAR PROCESSING (SPARE PROCESSORS NOT SHOWN)



function	subfunction	parts list	no. of parts	no. of identical functions	no. of parts	power consumption (W)	weight per function (kg)
input	ABI	semi custom chip glue chips 8Kx8 bits Cmos Ram	1 7 2	11	11 77 22	3.0 2.1 0.5	0.7
azimuth MCTM + RCTM	PBI	semi custom glue chips	1 7	23	23 161	6.6 4.4	22
	MCTM + RCTM	8Kx8 bits Cmos Ram	60	21	1260	1.9	
	cluster of 8 DSP's	TMS - 320 glue chips, Ram's, Rom's	8 80		168 1680	144.0 40	
deskew + output	ABI	semi custom glue chips 8Kx8 bits Cmos Ram	1 7 8	2	2 14 16	0.6 0.4 0.1	2
	cluster of 8 DSP's	TMS - 320 glue chips, Ram's, Rom's	6 80		12 160	5.4 2.0	
	output	glue chips	20		40	3.0	
TOTAL					~ 3650	~ 210	~ 25

Table 3 - Mass and power consumption budget (excl. mean Doppler processor)

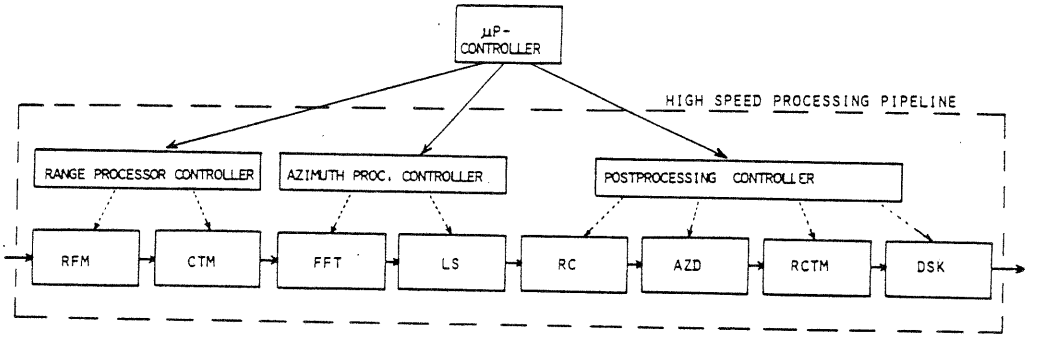


FIG. 2-1: BLOCK DIAGRAM OF AZIMUTH PROCESSING PIPELINE

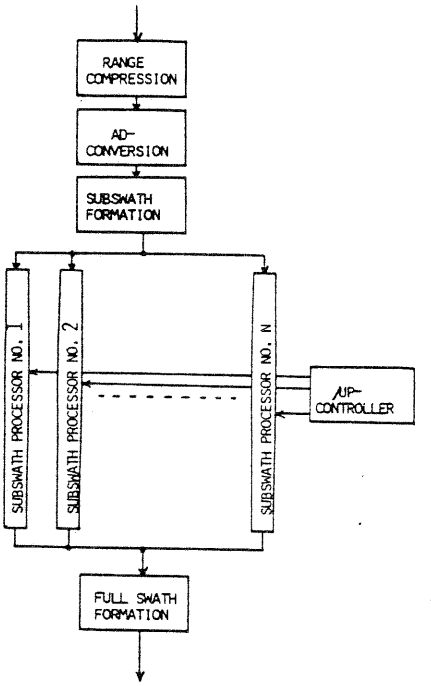


FIG. 2-2: BLOCK DIAGRAM OF FULL SWATH PROCESSOR.

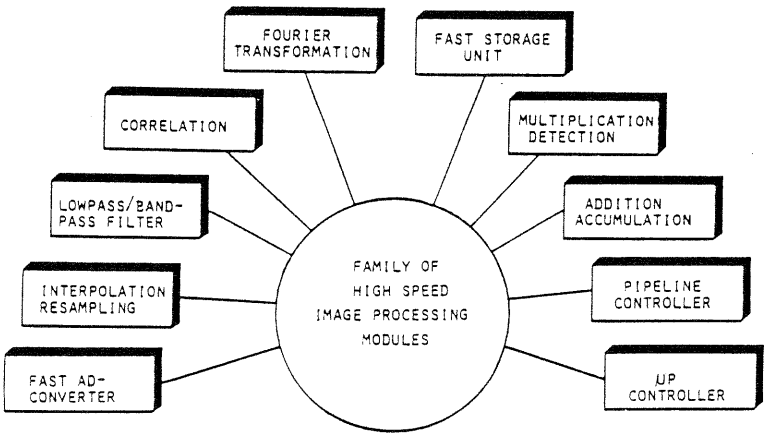


FIG. 3-1: FAMILY OF HARDWARE IMAGE PROCESSING MODULES.