EVOLUTION OF DIGITAL GROUND SAR PROCESSING SYSTEMS

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ABSTRACT

An increasing number of airborne and spaceborne Synthetic Aperture Radar (SAR) systems are used for a variety of remote sensing applications and more than 30 digital SAR processors have been developed worldwide since the launch of SEASAT.
Presently there are four types of digital SAR processors, existing or under development. Typical implementation concepts are:

- software on a general purpose computer, primarily used for algorithm development and experimental purposes
- software on a minicomputer augmented by array processor(s), used for experimental purposes as well as for operational tasks with low throughput requirements
- multiprocessor systems designed for high throughput operational processing
- hardware configurations for Real Time and Near Real Time processing

This paper presents the evolution of the different SAR processors in a retrospective view and describes the actual status of all known ongoing developments based on a survey, that was updated periodically over the last three years.
A cautious extrapolation of future processor development concludes the paper.

1. INTRODUCTION

The development of digital SAR processing technology for civil application has been triggered primarily by the first spaceborne L-band SAR carried on the SEASAT satellite. Although appropriate digital processing systems were not available during the lifetime of the satellite (Aug./Oct. 1978), shortly after several systems became operational and a variety of additional experimental systems have been developed meanwhile.

A first survey of SAR processors was presented by Guignard (1981) and updated later by Raney (1982) and Gredel (1982/83). The present paper finally concludes the series of updates with latest available information. It has to be seen in context with more detailed information prepared for this conference (Working Group II-5). More than 30 different processing systems from 16 organisations in North America, Europe and Japan are briefly characterized in terms of hardware configuration, algorithm, throughput and application. Future plans are mentioned and references are given.

The relevant information has been compiled from questionnaires that were returned from organisations known to develop or operate SAR processing systems.

2. SCENARIO OF SAR SENSORS

Beside the well known **SEASAT** L-Band SAR which acquired a unique data set during its three month life time in 1978, a Canadian aircraft **CV-580** with the ERIM X/L-Band SAR, upgraded by an additional C-Band channel, has flown a number of missions over Canada, Europe and Japan in the time frame 1981/83. This sensor will soon be replaced by the Integrated Radar Imaging System **IRIS**, a modern C-Band SAR sensor and processing system developed by MDA for operational use at CCRS. In addition to that an American airborne L-Band SAR has been flown for several missions on a **CV-990** aircraft operated by NASA/JPL.

NASA's Shuttle Imaging Radar **SIR-B** mission will be flown in September 1984 with an L-Band SAR which operates with different depression angles, variable data quantization and PRF, as well as in squint- and in spotlight-mode. The **SIR-C** mission is scheduled for 1987. A C-Band channel will be added to the SIR-B configuration. After the unfortunate failure of the X-Band SAR mode, as part of the Microwave Remote Sensing Experiment **MRSE** (an ESA/DFVLR experiment) on the first Spacelab flight, a reflight is planned for 1986. In addition to that the development of a C-Band SAR for the European Remote Sensing Satellite **ERS-1** in 1988 is in a phase-B-study, another C-Band SAR on **RADARSAT** is investigated in Canada for launch in 1990 and Japan plans to launch the **ERS**-satellite with an L-Band SAR in the early 1990's.

So in the future there will be several SAR sensors with a variety of operating modes carried on different platforms such as aircraft, Shuttle/Spacelab and satellite. All SAR sensors mentioned above provide or will provide digital data. The new SAR sensors are characterized by

- increasing complexity of SAR operating modes (e.g. SIR-B/C) and/or
- increasing data volume (e.g. ERS-1).

Therefore the digital SAR processors have to become even more flexible and/or provide Near Real Time processing capacity.

3. ALGORITHMS, PROCESSING SYSTEMS AND PERFORMANCE MEASURES

The digital processing of SAR data is a complex and for nearly all processor implementations also a time consuming task. The mathematical problem is a correlation. This sensor dependant one- or twodimensional correlation is executed by matched filtering, where a signal data matrix is convolved with a matched filter to generate the image data array.
The signal data matrix is formed by lines of sampled and digitized SAR pulse returns (range lines), successively stored in a signal memory with the columns representing azimuth lines. The matched filter is derived from the impulse response of the SAR system which depends on SAR parameters in range and sensor/target geometry and relative motion in azimuth. Considering full swath processing the typical processing array sizes for satellite SAR Systems are in the order of 10^8 samples for the signal matrix and several 10^6 coefficients for the matched filter. This results generally in datamanagement problems and in high computational load. The following algorithms are usually implemented:

1. Two-dimensional fast convolution **2DFFT**
2. Two times one-dimensional convolution executed as **R**ange **C**ompression followed by **A**zimuth **C**ompression **RC/AC** with the convolutions performed in either time domain or frequency domain or a combination of both
3. Spectral Analysis **SPECAN** after Range Compression

This is only a coarse classification of the different algorithms. More details are given by Bennett (1982) and Liu (1982).
The above mentioned algorithms are mapped on different hardware configurations to form the digital SAR processor. Some of them are used for experimental purposes, others perform operational processing. The hardware configurations can be categorized as:

- General purpose or large scale computer (type 1)
- Host computer with attached array processor (type 2)
- Multiprocessor system (type 3)
- Hardware implementation (type 4)

The performance of SAR Processors can be characterized in terms of:

- Throughput capability
- Image quality
- General aspects such as flexibility, automatic operation etc.

4. THE EVOLUTION OF SAR PROCESSING SYSTEMS

Table 1 contains an up-to-date list of all digital ground SAR processors and two airborne processors for civil application known to the authors. It lists 38 different processors from 16 organisations or companies in 7 countries. The information represents the status of March 1984. Compared to the first survey in 1981 this is an increase of more than 20 configurations. According to the classification of processors introduced above there are 6 systems of 'type 1', 23 systems of 'type 2', 4 of 'type 3' and 5 to 'type 4'. Not all of the processors are in use anymore.

The table lists for all processors the application, the basic algorithm, the type of processor and its status (which can be: in development, for experimental or for operational use) with a time schedule that shows the development and operational phases. The only performance parameter listed is the throughput primarily expressed as processing time for SEASAT images of differently sized ground areas. Even this gives only a coarse indication. More performance parameters are not mentioned for two reasons

1. All processors that use the same basic algorithm have small differences in their implementation, for instance the way to correct the range migration or the weighting of the reference function. In addition to that there are a present no generally agreed criteria for image quality which may be used for the comparison of all the different processors.
2. Many processors are known to produce images of adequate, good or high quality, so the main interest focusses in many cases on throughput enhancements, which is still a challenging task.

4.1 Medium and Large Scale General Purpose Computers ('Type 1')

It is evident that general purpose and super computers are very well suited for the development and experimental use of SAR processing algorithms. The software can be developed in high level languages and the system resources offer in general large memory and disk space thus reducing the severity of the data management problem. However, only very few 'type 1' processors have been developed so far. The only serious attempts can be reported from Japan.

Table 1. Survey on Digital SAR Processing Systems

Organisation		Processor	Application	Algorithm	Hardware-Configuration	Type 1	2	3	4	Throughput (hrs)	Time Schedule 79	80	81	82	83	84
JPL	1	IPD	S	RC/AC 1	SEL32/55,1xAP120		O			S: 100x100km/9.5	==========					
	2	IPDMX	S,CV-990	RC/AC 1	SEL32/55,3xAP120		O			S: 100x100km/2-3		====----------				
	3	Exp. S/P	S, I/r, Q/L	RC/AC 1	SEL32/77,3xAP120		E			S: 80x100km/<0.5			=====			
	4	SIR-B S/P	SIR-B,S,CV-990	RC/AC 1	SEL32/77,4xAP120		D			SIRB:50x100km/ 2				=======		
	5	Exp. S/P	S	RC/AC 1	VAX ,1xAP120		E			S: 16x16 km/ 1			=====			
	6	ADSP	SIR-C	tbd.	spec. HW				D	SIRC: tbd.						==
JHU/APL	7	Exp. S/P	S	RC/AC 1	VAX11/780, AP164		E			S: 100/100km/5.6			======			
MDA	8	SEASAT	S	RC/AC 1	PE 8/32, 1xAP120		O			S: 40x60 km/ 8	==========					
	9	GSAR	S,MRSE,CV-580	RC/AC 1	PE 8/32, 1xAP120		O			S: 75x100km/23		========------				
	10	CV-580 RTP	CV-580,Q/L,I/r	timedom.	spec.HW/8086Micro				O	CV580:6km swath r/t		====----------				
	11	IRIS RTP	IRIS, Q/L	timedom.	spec.HW				D	IRIS: r/t			=======			
+ Dornier	12	Breadboard	ERS-1,Testdemo	SPECAN	PSPE spec. HW				DE	ERS-1:20km s/s r/t			==========			
CCRS	13	SEASAT-S/P	S	RC/AC 1	PE 3240, 1xAP120		O			S: 40X60 km/ 8		--------				
	14	Exp. S/P	S, I/r, Q/L	RC/AC 1	DEC 10/90	E				S: 100x100km/33	=======					
	15	GSAR Proc.	S,CV-580	RC/AC 1	PE 3240, 1XAP120		O			S: 75X100km/21			----------			
CRC	16	CRC-S/P	S,CV-580	RC/AC 2	PE 8/32, 1xAP120		O			S: 21x47 km/ 9		----------				
	17	CRC-MKII-S	CV580/airb.SAR	RC/AC 1	PE 8/32, 1xAP120		O			HRNS: 5.8x2.9/ 1			==========			
RAE/SDL	18	ESPF	S,CV-580	RC/AC 3	PRIME750/2,1xAP120		EO			low throughput	==========					
Marconi	19	S/P	airb. SAR	timedom.	spec. HW				EO	1.37MEG multip./sec		======				
DFVLR	20	S/P MDA	S	RC/AC 1	PE 8/32, 1xAP120		O			S: 40x60 km/ 8		--------				
	21	GSAR Proc.	S,CV-580,MRSE	RC/AC 1	PE 3252, 1xAP120		O			S: 75x100km/15			----------			
	22	GSAR Proc.	SIR-B, MRSE	RC/AC 1	PE3252, AP120/ST100		D			tbd				=====		
NDRE	23	S/P	S	RC/AC 1	NORD 100/NORD 50		E			S: 45x55 km/40		========--				
	24	Multi Proc.	ERS-1	RC/AC 1	Host + spec. HW			D		ERS-1: near r/t			==========			
Telespazio	25	EMMA-M/P	ERS-1	RC/AC 1	VAX+EMMA Multiproc.			ED		ERS-1:100x100/12min						===
NEC	26	S/P	S	RC/AC 1	ACOS 77/NEAC 700		E			S: 17x30 km/25		====				
	27	S/P	S	RC/AC 1	MS50/1xAP120		E			S: 32x45 km/ 8			=======			
	28	NEDIPS	S	RC/AC 1	MS50 + TIP's			ED		S:50x100/4/2<10min			==========			
Mitsubishi	29	S/P	S	RC/AC 1	IBM 370/CRAY-1	E				S: 20x10 km/ 1			=======			
	30	S/P	S,CV-580	RC/AC 1	COSMO 700/AP-120		E			S: 17x20 km/ 5			=====			
	31	S/P	tbd.	RC/AC 1	COSMO 700/+n x MSP			ED		tbd.				====		
Hitachi	32	S/P	S	RC/AC 1	HITAC-M200	E				S: 17x60 km/15			====			
	33	S/P	S	RC/AC 1	HIDIC80/AP120B		E			S: 17x23 km/1.2			=====			
	34	S/P	S	RC/AC 1	HIDICV90/50/AP120B		E			S: 40x50 km/2.5			========			
Fujitsu	35	M-SAR/F	S	RC/AC 1	M-170 F	E				S: 90x100km/32						
	36	M-SAR/F	S, CV-580, ERS	RC/AC 1	FACOM/M-380	E				S: 90x100km/3.5				====		
	37	S/P	S, ERS	RC/AC 1	VP-200/M-380	ED				S: 90x100km/<12min				=====		
RRL	38	S/P	S,SIR-B	RC/AC 1	MS-50/1xAP120		E			S: 45x75km/4.25					=========	

S/P = SAR Processor, E = Experimental, O = Operational, D= in development, RC/AC = Range/Azimuth compression (1=2x1dim. FFT 2=2dim. FFT, 3=AC in time domain), Q/L = Quick Look, I/r = low resolution (ca. 100 m), S = SEASAT, r/t = realtime, s/s = subswath, MSP = Mitsubishi Signal Processor, M/P = Multi Processor, ==/-- development/operational phase, RTP = Real Time Processor

At Mitsubishi (Ono, 1982) there was a SEASAT SAR Processor implementation on an IBM 370/CRAY-1 configuration equipped with 0.5 MWords of memory. The software was developed in FORTRAN. The initial processing time achieved was 1 hour for a 10 km by 20 km area and was gradually improved to 15 min for a 17 km by 20 km area. Estimates were made that predicted 10 to 30 minutes processing time for a full swath image. Before the throughput potential was fully exploited the software was transferred to a 'type 2' configuration (Ono, 1983) as an intermediate step to a 'type 3' system that shall include several signal processors under development at Mitsubishi.

The only 'type 1' configuration left is the most recent development of a fairly generalized FORTRAN 77 software package by Fujitsu (Sekiya, 1983) on a medium scale computer M-170 F with 32 hours processing time for a 90 km x 100 km SEASAT image. Transfer to a large scale computer reduced the processing time to 3.5 hours and installation on the supercomputer VP 200 (533 MFLOPS, 256 MByte main memory and vectorizing compiler) further reduced the processing time to 12 minutes (Kosaka, 1984). This is by far the fastest SEASAT processor and it demonstrates clearly that the new generation of Supercomputers is capable of Near Real Time SAR Processing.

However, the disadvantage of such implementations is the high investment and operational cost and the fact that such machines can normally not be used as dedicated systems.

4.2 Host Computer with Attached Array Processor(s) ('Type 2')

The widest spectrum of digital SAR processors are those implemented on 'type 2' systems. The typical configuration is depicted in Figure 1.

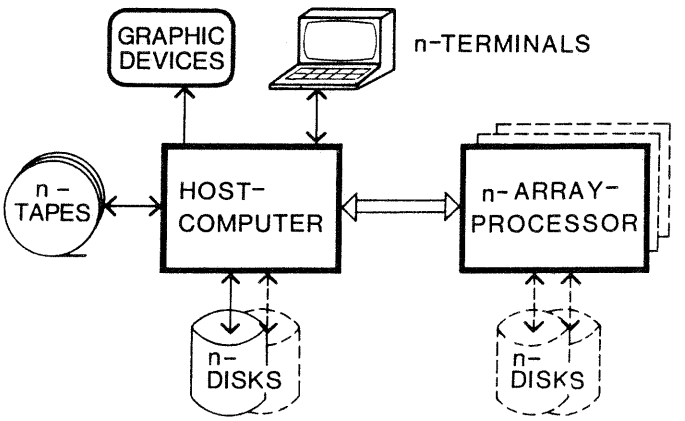

Figure 1. 'Type 2' Digital SAR Processor

The system consists of a hostcomputer with standard peripheral devices augmented by one or several array processors. Host computers are generally powerful 32 bit minicomputers with several MBytes of memory, tape input and 300-Mbyte-disk drives. There is a variety of different host computers represented while the array processor used in nearly all cases is the well known AP120B from Floating Point Systems with 10 MFLOPS computational rate. The implementation makes generally use of the large data arrays residing on host computer disk. The basic vector operations, which are fast convolutions, are realized mostly in the frequency domain and executed on the array processor.

The initial system developments took place in 1978 by MDA (Bennett, 1979), JPL (Wu, 1980), CRC (Vant, 1979) and RAE (Corr, 1978). The MDA software is

also used by CCRS (Princz, 1982) and DFVLR (Gredel, 1982). Soon after the availability of digitally processed SEASAT images, similar developments were started by the Japanese industry and led to comparable configurations.

With only two exceptions, the basic algorithm used is Range Compression followed by Azimuth Compression, both operations performed in the frequency domain. However, there are many differences in the way the range migration is corrected, the looks are extracted, the data are quantized and resampled from slant- to ground-range. The exceptions are the RAE processor which performs the azimuth compression in the time domain (resulting in lower throughput capability) and the first CRC-processor which is the only processor with a two-dimensional convolution implemented. This design was driven by requirements to process data of an airborne squinted SAR. An interesting RC/AC alternative for squinted SAR's has been developed recently (Vant, 1983).

Initially all SAR processors were developed to process only data of the SEASAT L-Band SAR. Most of them included beam tracking (clutter lock) routines to refine the attitude data. With the availability of airborne multi-frequency SAR data from the Canadian CV-580 aircraft some processors became more flexible. Autofocus routines were added in many cases to precisely estimate the sensor velocity from the data. 'Beam tracking' and 'autofocus' allow autonomous processor operation without a need for accurate orbit and attitude information.

The throughput of the 'type 2' configurations was initially in the order of 10 to 100 hours for a full swath SEASAT image. Today this varies from 3 to 30 hours, where the fastest implementation still is the JPL processor which has now three AP120B' attached to its SEL 32/77 host computer (Barkan, 1981) and will interface a fourth unit for SIR-B data processing.

The 'type 2' configurations are the only configurations that were ever used for operational processing of SAR data (SEASAT, CV-990 and CV-580). This was done at JPL, CCRS, RAE and DFVLR. However, in view of the future satellite SAR sensors, the present 'type 2' configurations are not capable to meet the processing demands, which at least require 'no backlog' processing. This requires a 10 to 100 times better throughput performance.

The present 'type 2' implementations have no significant growth potential. This is primarily related to fact that in nearly all installations the host computer is completely involved in all data transfers between host disks and attached vector processor. As the computational rate of the array processor increases, the addition of array processors makes the SAR processor to become I/O-bound. The solution to this problem is to completely transfer the algorithm to the array processor and attach private disks. Such a configuration was recently implemented at JHU/APL (Raff, 1983) on a VAX 780/AP 164 configuration with four disk drives. The VAX only provided data input/output via tape. The AP 164 has an increased wordlength, more memory but the same computational speed compared to the AP 120 B. Without any tuning the processing time for a 100 km x 100 km SEASAT image was 5.6 hours.

A similar concept was analysed recently by DFVLR. It was found that a new generation array processor (ST100 from STAR Technology with 100 MFLOPS) with high speed and high capacity disk drives (10 MByte/sec block transfer rates) and direct raw data input, an ERS-1 full swath image can be generated in 15 minutes. The host computer then only performs control functions. The realisation of this concept started at DFVLR.

4.3 Multiprocessor System ('Type 3')

General Multiprocessor architectures for SAR processing have been reviewed by Guignard and Jones (1983). The term 'Multiprocessor System' used here is restricted to the configuration: supervisor/controller system (in most cases a minicomputer) organizing several or many dedicated processor systems, structured within a network.

The 'NEDIPS SAR Processor' developed by NEC (Ito, 1982) is somewhere in between a 'type 2' and 'type 3' processor. A host computer controls a Template Image Processor (TIP), a high speed memory and disks. The TIP's contain operational units on a circular pipeline reaching a computational performance of 48 MFLOPS and have to be seen as 'data flow' system.

The implementation of the RC/AC Algorithm in the frequency domain is already capable of processing SEASAT full swath images in 4 hours. The projected performance of a NEDIPS with several enhanced TIP's working in parallel or in sequence should allow to process a full swath image in less than 10 minutes.

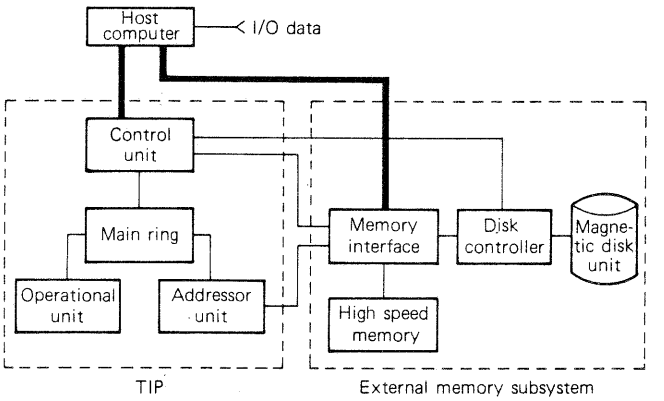

Figure 2. NEC SAR Processor using NEDIPS

The 'NDRE Multiprocessor' (Norsk Data, 1982) is a network of data buses, supervisor buses for control, signal processors, memories and disks controlled by a minicomputer as control processor. With a MARS 432 from Numerix as signal processor, different configurations were analysed that should be capable of processing an ERS-1 frame in 8 to 30 minutes. The algorithm used is the well known RC/AC mapped on a rather complex, but fully programmable

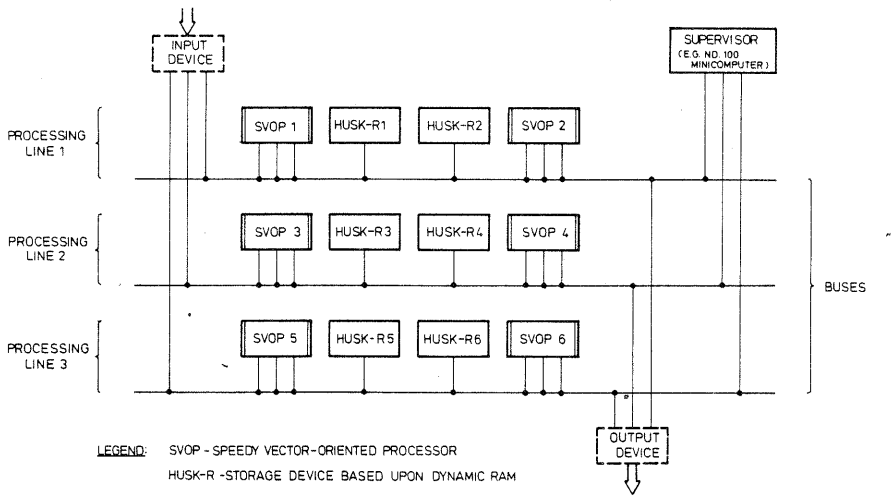

Figure 3. NDRE Multiprocessor

hardware structure which is based on an earlier developed general concept, called 'Martinus'. A specific high level programming language HOLM has been created and will support user's system application.
Two further 'type 3' configurations are under planning in Japan and Italy. Details are not yet available.

4.4 Hardware Implementations ('Type 4')

The 5 'type 4' configurations in Table 1 are strongly hardware oriented and designed to generate images at Real Time or Near Real Time rates.
The three processors for airborne SAR sensors are special hardware devices with Range and Azimuth Compression performed in time domain. Two realtime processors - developed by MDA - are used onboard for quick look and navigation support for the CV580 X-Band SAR (Bennett, 1979) and the IRIS C-Band SAR (Bennett, 1983). The Marconi processor is a groundbased quick look processor. Two processors are operational, one is nearing its completion (IRIS). None of these processors is capable of processing satellite SAR data.
In addition there is one system under development for Near Real Time processing of satellite SAR sensors. The 'ESA/ESTEC SAR Processor and Test Facility (Breadboard)' wich was developed by MDA/Dornier (Okkes, 1983) is depicted in Figure 4. It is a system that demonstrated already Near Real Time processing capability for the linear range migration correction and the azimuth compression task of 1/5 subswath assuming nominal ERS-1 parameters. This Breadboard is a microprocessor controlled pipeline of Programmable Signal Processing Elements (PSPE) and a corner turn memory. It is the only implementation that uses the 'Spectral Analysis' algorithm which restricts the processor more or less to multilook processing of C/X-Band satellite SAR sensors. Based on this design a Fast Delivery Processor and a Quick Look Processor with reduced resolution were projected for the ERS-1 C-Band SAR with throughput estimates of 1/20 and 1/6 of real time respectively.

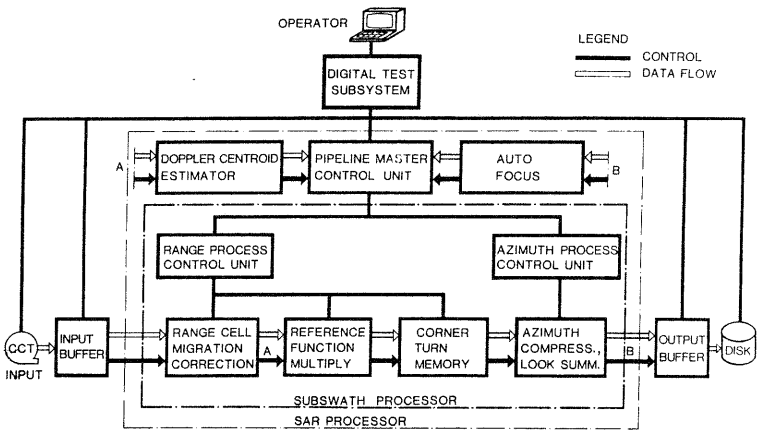

Figure 4. ESA/ESTEC SAR Processor and Test Facility

According to a private communication by Curlander, JPL is planning to develop an 'Advanced Digital SAR-Processor ADSP' on new hardware technology to overcome the demanding processing problem for the SIR-C sensor in 1987.

5. CONCLUSION

SAR Processing capabilities have been developed by 16 different groups in 7 countries. In view of future SAR sensors on Shuttle and satellites, it is expected that even more groups will be involved due to the fact that more work on the interpretation of SAR data will be done. This requires a full understanding of the SAR image formation process and in many cases it might even require an application-dependent control over the processor.
It is assumed that the 'type 1' and 'type 2' processors will be further used in the future primarily for experimental purposes and that the enhancement work will concentrate more on image quality than on throughput. It is further assumed that the percentwise relationship between 'type 1' and 'type 2' processors will not change significantly in the future because the experimental work requires a high degree of interaction with image display and processing capabilities and not many groups have access to a supercomputer.

The 'type 3' and 'type 4' processor developments are primarily driven by operational requirements of ground segments for satellite SAR sensors. For several years such systems seem to be the only alternative for high throughput SAR processing. However, recent studies have shown that enhanced 'type 2' processors with latest available technology can become competetive.

The authors wish to express their thanks and acknowledgement to all people who contributed information on their processing systems in a cooperative manner, thus enabling the preparation of this general survey. Additional details on the systems will be prepared for WG II-5.

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7. ABBREVIATIONS

CCRS	Canada Center for Remote Sensing
CRC	Communications Research Center (Canada)
ESA	European Space Agency
ERIM	Environmental Research Institute Michigan (USA)
GSAR	Generalized SAR Processor (MDA)
JPL	Jet Propulsion Laboratory (U.S.)
JHU/APL	John Hopkins University/Applied Physics Laboratory (U.S.)
MDA	McDonald, Dettwiler and Ass. (Canada)
NDRE	Norwegian Defense Research Establishment (Norway)
NEC	Nippon Electric Company (Japan)
RAE	Royal Aircraft Establishment (U.K.)
RRL	Radio Research Laboratories (Japan)
SDL	System Designers Ltd. (U.K.)