COMPONENTS FOR VIDEO-BASED PHOTOGRAMMETRY OF DYNAMIC PROCESSES

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ABSTRACT

Applying photogrammetric discipline to outstanding problems in the measurement and control of dynamic processes enhances the prospects for "precision 3-D intelligence". Real-time digital image processing is fundamental to such an endeavor. The status of image acquisition and processing hardware as component parts in video based solutions for close range photogrammetric control of dynamic events is reviewed, with reference to experience at NRC.

1. INTRODUCTION

The outlook for photogrammetric measurement and control of close range dynamic events has never been more promising. "Superchip" imagers, processors and memory are leading to the solution of outstanding problems in real-time, in-situ, filmless photogrammetry, imaginatively and cost effectively. As huge rooms full of vacuum tubes gave way to tiny silicon chips, traditional chemical imaging systems are giving way to CCD's, array processors and disk storage. This cannot help but have a profound impact on the way photogrammetric solutions are implemented, and on the scope of applications.

With electronic imaging as the basis, automated inspection systems are in wide use, and robots with machine vision are poised to make expensive fixturing equipment obsolete in manufacturing. In spite of nearly 50 machine vision system suppliers, no 3-D system for general application is commercially available, Kent, 1986. This lack clearly invites photogrammetric expertise.

The technology is changing so rapidly that one cannot pretend to convey more than a snapshot of where the burgeoning field of electronic image processing is. This paper attempts this task as it relates to fast, cost effective, hardware for application to close range photogrammetry. A substantial portion is devoted to image sensing and acquisition because of its importance, followed by a section on real-time image processors. Image acquisition and processing phases are frequently sufficient for many real-time close range problems because the needed output is a decision strategy and signals to either control a 3-D process or derive a conclusion from it. Image display and archival storage are not paramount issues in such applications. A companion paper, Real, 1986, deals more directly with aspects relating to visual communication, where the human eye is the prime receiver of the output from the video system, as opposed to an output consisting of automatic decision and action signals based upon electronic images as input. Some appended results from the author's institution complete the paper.

2. ELECTRONIC IMAGE ACQUISITION

Electronic image acquisition consists of a means of photosensing, sensor addressing, analog to digital conversion and electronic image storage. Solid state matrix cameras, popularly called "CCD" cameras, have assumed a preeminent position as the natural transducer for optical input to a computer, since image information is sensed and spatially quantized from a metrically stable, miniature, rugged device. A brief history, description and appraisal follows.

2.1 Image Sensors - Electron Beam

Image acquisition by photo-electronic means, dating sixty years back to the ionoscope, has evolved through a series of devices. The most common sensor in every class of television camera has been the photoconductor imager comprising one of, (Flory, 1985):

Antimony trisulphide,
Lead oxide
Saticon (TM - Japan Broadcasting Corp.)
Newvicon (TM - Matsushita Electrical Industries)
Silicon diode array

Although photoconductor camera tubes have become known generically as Vidicons, (large camera, Fig. 1b), initially this term referred only to a tube having an antimony trisulphide target. A second class of sensors, called "electronic imaging sensors" is characterized by an image section in which electrons are emitted when photons are incident, and a second plane from which the focused electrons may be scanned. The Image Dissector, Orthicon, Isocon and Silicon Intensifier Target Vidicon fit into this class. The above devices require an electron beam to address (scan) the sensor and because of this the assembly is housed in a vacuum environment. It is the analog nature of this sensor address system which imposes spatial and photometric accuracy limits overcome by the third sensor category, solid state sensors. Note that the above sensors are also "solid state", but the photo charge sampling and transfer system is not.

2.2 Early Solid State Imagers

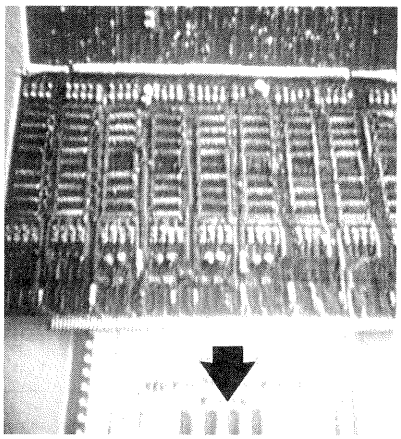
Silicon was suggested as a vidicon target material in the 1960's. A single crystal wafer of n-type silicon 10-20 μm thick is supported behind a glass faceplate which contains the vacuum tube. An array of diodes is formed on the beam incident side of the wafer. Photo generated charge carriers originate in the wafer and holes move into the diode p-region. The diode capacitance stores the charge until the scanning beam replaces the electrons lost in the diode, and this current is read as the video signal. The diode array is fabricated on 14 μm centers by traditional transistor techniques. In essence then, one step in the evolution to the solid state camera existed in the tube technology. The leap to the true solid state camera was gained by solving the addressing and charge transport scheme with solid state design.

The potential of the self scanned solid state imaging sensor languished until the aerospace age imposed its need for a small, rigid, low power, high reliability video camera. Most solid state cameras since have been fabricated in silicon because of the highly developed technology of this material and its low lag. The first fully electronically scanned solid state image converter system was a 50×50 pixel phototransistor array built in 1965, Strull, 1972.

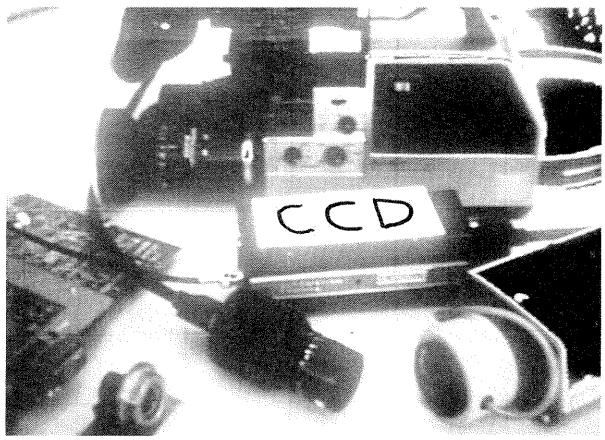
Silicon is not an ideal visible light sensor because of its high near infrared response. This very response is the basis for many surveillance applications. Neither is it a good ultra violet sensor, although state of the art optimization has yielded a response on the order of 50% at 300 nm. One of the most exciting attributes of the solid state imager for photogrammetrists is having a two-dimensional array of sensors metrically stable in both time and space. That they are also high in sensitivity, dynamic range, miniature, rugged and reliable are bonuses.

Solid state matrix cameras came to be known popularly as CCD (charge coupled device) cameras even though area imaging arrays were fabricated in the 1960's using phototransistors, Schuster, 1966, and CdS field effect transistor technology, Weimer, 1969. These devices suffered from response nonuniformities and other forms of spatial noise associated with X-Y readout techniques. The charge coupled device (CCD) concept, Boyle, 1970, is unique in its ability to mix low power, high density functionality for a variety of uses on a single chip. Imaging, analog and digital memory and processing can be integrated together, as indeed they were in an interesting imager with integral 3×3 convolver, Hall, 1979. The author utilized non imaging CCD

functions dating back to 1976. A 1.31 Mbit solid state memory system, the first commercial bulk one of its kind, consists of 16 Kbit CCD memory chips on a 30 cm × 38 cm board, Fig. 1a, (a second control board for it is in the background; a substantial system manual in the foreground). The four small dark rectangles at the base of Fig. 1a are 256 Kbit memory chips, currently in vogue, providing a 1 Mbit memory at 0.5% of the cost of the other; say nothing of reduced space, power consumption and high speed. The author has also used CCD analog correlator devices before superior digital ones displaced them in 1980.



a



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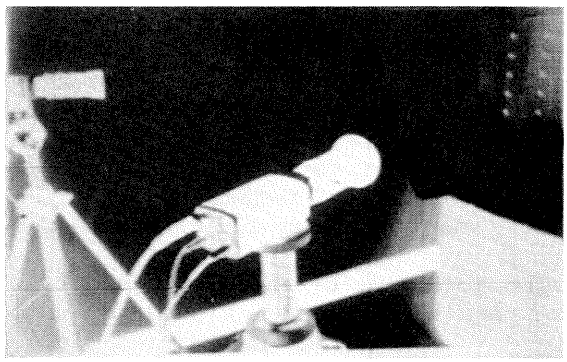

Fig. 1

(a) 1976 - 1.31 Mbit CCD memory board.
1986 - 256 Kbit memories (arrow).
(b) Vidicon and CCD cameras.
(c) X-Y CMOS cameras.

An earlier 100×100 pixel CCD imaging chip (Fairchild) is mounted on a circuit board on the left side of Fig. 1b, shown with a more recent 380×488 pixel interline CCD camera (Fairchild, center Fig. 1b) mounted integral with a lens and connected to the remainder of its electronics by cable. To the right in Fig. 1b is one of the first standard TV CCD cameras (320×512 pixels from RCA, 1981). Fig. 1c contains the silhouettes of two Hitachi X-Y MOS 320×244 pixel cameras used with a commercial real-time image processing system, El-Hakim, 1986.

2.3 Solid State Imagers Today

Compared to the usual pace of integrated circuit development, reasonably priced, quality, TV size solid state imagers (typically 400H×500V pixels) were a long time in coming after their announcement as early as 1971, Strull, 1972. Unlike other very large scale integrated devices such as memories, where redundancy is added and used if part of the chip tests faulty, imagers had to be "perfect". Yields were low, costs high and all had blemishes, the degree of which determined their price. A relatively blemish free chip cost thousands of dollars a few years ago. Yields and quality improved so that, today, T.V. color imaging chips of one hundred dollars are in sight - Electronics, 1986.

For years the trade-off between solid state imaging devices has been inconclusive, dependent upon the ingenuity of the device designer on the one hand, and the application on the other, with no clear winner in either the commercial TV or industrial market, Carter, 1985. Thus, four main types of solid state sensors coexist as follows. (Photosite sizes range from approximately 12 µm x 12 µm to 55 µm × 55 µm, depending upon format size and manufacturer),

CCD	INTERLINE	*Fairchild, Sony
	FRAME	RCA, EEV, VSP
CID (charge injection device)		General Electric
PHOTODIODE	- MOSFET	Reticon, Hitachi

(*There are in excess of thirty suppliers of solid state cameras. These listed are for example only and does not indicate endorsement.)

Photodiode arrays emerged some two decades ago in response to aerospace requirements and still serve well. Typically they are X-Y addressed with a MOSFET (metal oxide silicon field effect transistor) gate connected at each crossing point, Flory 1985. Its production lends itself readily to manufacturing using very well established CMOS processes in the integrated circuit industry.

The charge-injection device (CID) has nearly contiguous photo sites (pixels) in both directions and has been used extensively in astronomy, the first scientific discipline to utilize solid state imagers, Gutshall, 1981. It has also been used in a 32 band multi spectral pushbroom scanner, Stewart, 1985. An advantage of this imager is its inherent noise reduction feature because the signal can be transferred to the read capacitor and then transferred back to the integrating elements without altering the integration. Such a nondestructive read feature is unique to the CID, where the charge is injected into the substrate after each integration period. It also exhibits a superior anti-blooming characteristic.

Charge coupled devices (CCD) belong to a more general class called charge transfer sampled analog devices. From its introduction, Boyle, 1970, the most promising use has been in imaging arrays, both linear and area. Literature abounds on this subject to the extent that the term "CCD" is almost synonymous with "solid state camera" in spite of it being only one class of solid state imager, and even though CCD is a versatile technology with non imaging attributes mentioned previously. Charges, induced as a result of photon irradiation, Fig. 2a, are stored in cells under an electrode. An appropriate phased sequence of potential shifts from a clocking system is capable of moving the charge along a row of electrodes with little loss. Thousands of transfers may take place before the loss is significant. The "image", in the form of sampled analog potentials proportional to the photon induced charges, is mapped from the array serially through a register onto a single video line where it is read out one pixel at a time. Usage of the term "digital camera" is misapplied, since the sensor and the transfer system is sampled analog in its nature. The output cannot be read by a computer before converting the sampled analog signal into digital form by a device fabricated using a separate technology.

CCD's are either interline, Fig. 2b, or frame (field) transfer devices, Fig. 2c, Flory, 1985. Claimed advantages and disadvantages of the past are no longer valid, making predictions hazardous. Problems such as blooming, smear, blemishes (partially or non-operating pixels) and pattern noise are being improved, and may, in future, cease to be issues in many applications. However it is beginning to appear that the scales are tipping in favor of the frame transfer device. Its photo sites are nearly contiguous in both directions, an important consideration for quality imaging. Since it makes the most efficient use of the imaging area (approximately half of the sensing area of the interline device is devoted to the transfer process, hence is masked in columns so as not to be light sensitive) this advantage can be used to produce superior resolution, improved sensitivity or smaller chip area. Indeed, a recently announced 2048×2048 pixel imager (Tektronix) is a frame transfer device, Blouke, 1985. The frame transfer sensor seems to combine and improve upon the good features of the others, and with a smaller chip area, therefore also has the potential cost advantage

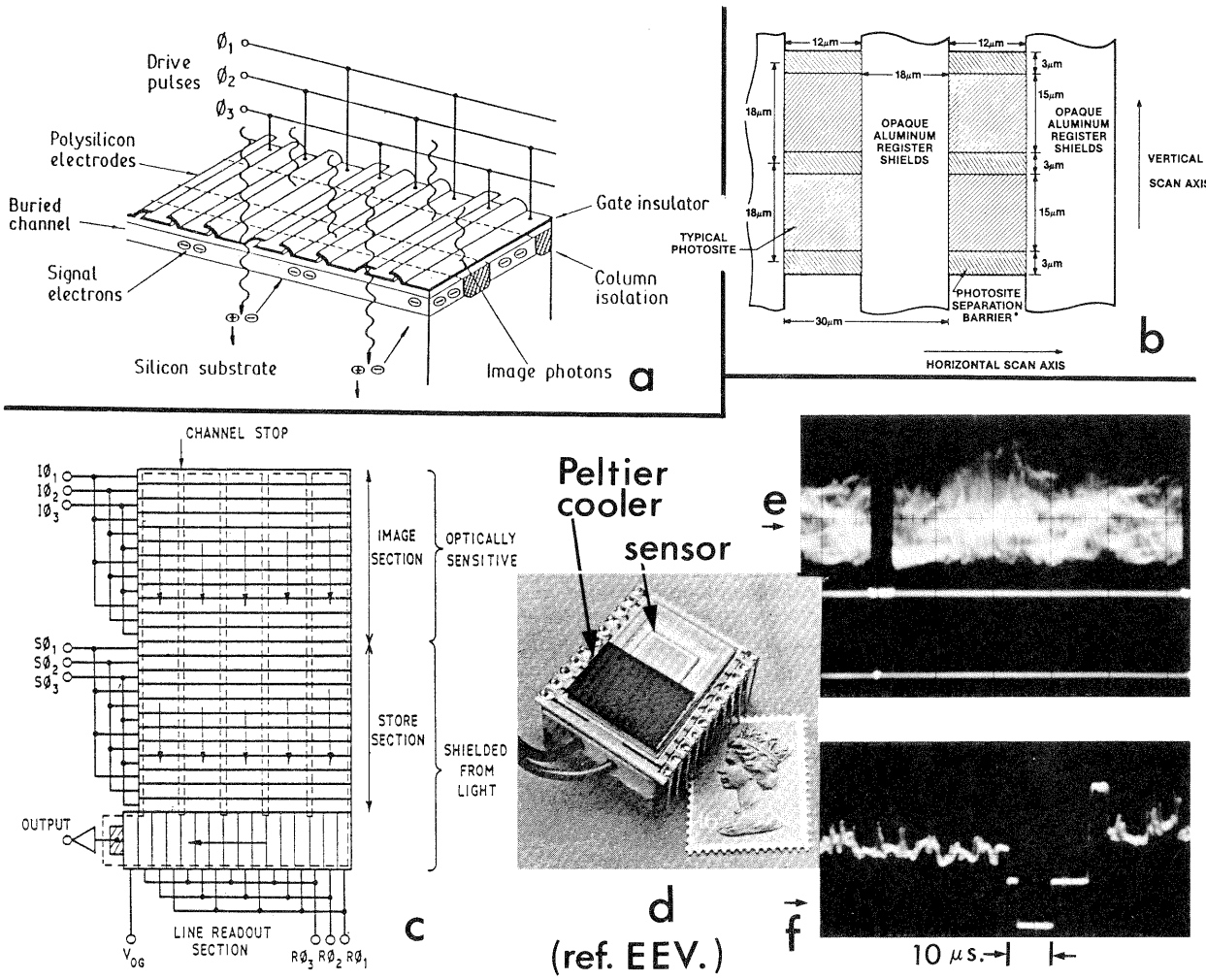

Fig. 2

(a) Section of CCD image sensor.
(b) CCD interline imager.
(c) CCD frame transfer imager.
(d) CCD frame-transfer imager with integrated Peltier cooler.
(e) Composite video signal.
(f) Detail of video line signal.

as well as quality advantage. The ease with which electronic shuttering and device cooling, EEV, 1984, Fig. 2d, for noise reduction may be incorporated into this device is important in the photogrammetric context.

Issues in camera design for visual communications are not necessarily the same as for robotics type applications, for example, where high frame rate and low cost may take precedent over a large sensor format with superior noise specifications. Parameters such as noise, dynamic range, linearity, collection and charge transfer efficiencies and price influence which camera is chosen for a particular task. The range of possible tasks in close range photogrammetry is large, so it is fortunate that there is a growing choice of solid state camera designs for varied purposes. Scientific solid state camera design is only now reaching importance, kept in the background by the race for supremacy in the high volume consumer and industrial market. Scientific solid state camera development is discussed elsewhere, Real, 1986. Noteworthy of past special designs for scientific application are the 800×800 pixel camera (Texas Instruments) for space exploration, Norris, 1981, and Kodak's 2000 frame per second camera for capturing fast events, Lee, 1982. (A commercial version of the latter is being marketed as of this year under the name Ektapro.)

2.4 Analog to Digital Conversion (ADC); Image Frame Grab and Storage

The ease with which solid state cameras are utilized belies their analog circuit complexity. Although the digital camera concept is compelling, much of the circuitry required external to the imaging device is analog in nature. The output video is a clamped composite sync./video signal, Fig. 1e, where the video component is a sampled analog voltage not exceeding 1 volt peak to peak. The accumulated charge from each photo site emerges in turn as a voltage proportional to this charge, minus charge transfer loss, corrupted with possible transfer noise and altered by possible internal filters. During each pixel time slot (approximately 130 ns for a 400×500 pixel array) the output voltage is held constant after sampling by a "sample and hold" circuit, so that the output voltage has a staircase quality to it. The video signal emerging for processing is the result firstly of spatial sampling, defined by the particular geometry of the photo site array, and secondly by whatever analog signal conditioning that occurs (amplification, prefiltering, sample and hold) between the imager and the camera's video output port. Part of one video line with horizontal sync. signal is shown in Fig. 1f.

A separate device, fabricated by a completely different integrated circuit process than the imager, performs the conversion from analog voltages to their digital representation. It was not until 1978 that the single chip video rate "flash" analog to digital converter was born, Wilson, 1986, providing a miniaturized, cost effective solution to the problem. To this day, ADC conversion (and to a lesser extent, digital to analog conversion, DAC) is a demanding art, Wilson, 1986. Differential linearity, straight-line linearity, "glitches", bandwidth, noise and threshold are factors in their specification and design. Today there is a choice of quality flash ADC's up to 200 MHz bandwidth and to 13 bits of resolution. They do exist to higher resolution, but at sub video rates (i.e., 16 bits, 1 μs conversion rate).

Image frame grab and storage complete the image acquisition sequence for an image processor. "Frame grab" may or may not include digital memory for the image, depending upon the wording used by the vendor. If not, "frame grab" will include the ADC, clocking and synchronizing circuitry to store one video frame in one frame time (1/30 sec. for standard NTSC TV, 1/25 sec for CCIR TV). Not only must the ADC be fast, but the memory also, which is why large video RAM (random access memory) has been, until recently, a significant expense, (64 Kbytes for a 256×256 pixel image, 256 Kbytes for 512×512 and 1 Mbyte for 1000×1000). If ADC and/or memory is too slow, the image will have to be stored over a number of frames by storing every n^{th} pixel per unit time. (i.e., If the ADC-memory combination is only half as fast as the video rate, odd pixels are stored over one frame first, then even during the next.) Having a frame store greatly increases the flexibility of an image system. Once the "snapshot" is captured, subsequent processing may proceed at any pace. Only in rare cases can a system be designed where image processing algorithms are fixed a priori and the processor is sufficiently fast to perform its function on the video image "on the fly" without a frame store. Frame grab units usually have three digital to analog converters (DAC's) for driving the red, blue, green (RBG) inputs of a color monitor from color look-up tables. Single circuit boards today may contain ADC, DAC's, one or more frame memories, arithmetic processors, control and clocking circuits at a relatively low price ($3,000 U.S.), Sullivan, 1984. The 64 Kbit memory chips, standard until recently, are yielding to the 256 Kbit ones. 1 Mbit chips are available (not yet price competitive) while 4 Mbit memory chips have been demonstrated. Lurking behind these very high densities has been a debate about their error rate integrity, Bursky, 1983.

It seems certain that the photogrammetric community can look forward to both the multi mega pixel solid state imager and the multi megabit memory chip becoming standard components. Even personal computers can be enhanced with ever more powerful image coprocessing options capable of frame grabbing up to 1024×1024 pixel images and performing multi-point image processing algorithms in sub second times, Tetewsky, 1985, Allen, 1986. The improved choice and power of specialized chip level digital signal processors will provide opportunities for integrating digital image processing capabilities right into the video camera.

3. REAL-TIME IMAGE PROCESSORS

Real-time image processing has given computers the ability to monitor and control dynamic information, making possible wonders ranging from a robotic tree fruit harvester to automatic machine assembly from bins of parts, Casäsent, 1985. It goes without saying that the fusing of solid state imaging technology with electronics is imparting profound changes to an extent not yet fully imagined. Unsolved problems in 3-D measurement and control require the merging of fast photogrammetric algorithms with techniques in image transformation and reduction (low-level) and image understanding (high-level) processing. Hardware for the former is discussed as preprocessing components for "precision 3-D intelligence."

"Real-time" implies digital image processing at the video rate of 30 standard TV frames per second or the equivalent (i.e., 120-256×256 pixel images per second, the size often used in machine vision for computer integrated manufacturing). Depending upon the vendor, this term may only apply to the simpler single point image processing algorithms, while the remainder function at "near real-time". Where speed is the issue, special hardware is still the only solution in most applications, although low cost general purpose digital signal processing chips are constantly improving in speed and functionality.

Processing algorithms are as diverse as the potential applications, but fast image operations associated with today's advanced image processors can include any combination of the list in Table 1.

Table 1 Common Image Operators Implemented by Coprocessors

1. Arithmetic (single point)
   - 1.1 Single data set
     - 1.1.1 Shifting, thresholding, clipping, normalization.
     - 1.1.2 Transform via look-up table (LUT).
   - 1.2 Combination-multiple data set
     - 1.2.1 Add, subtract, multiply, divide.
     - 1.2.2 Test for equality-matching.
     - 1.2.3 Overlays (graphics, images, text).
2. Neighborhood (multi-point)
   - n×m convolution filtering for digital implementation of low, high or band pass spatial filtering.
3. Statistical
   - histogram equalization and specification.
4. Geometric
   - scaling, translation, rotation, warping and resampling.
5. Correlation; Fourier Transform
   - image search, matching and locking.
6. Morphological Operations
   - image reduction and description for computer analysis and "understanding."

Table 1 is by no means exhaustive, but includes those operations for which some form of dedicated processing (hardware with microcode in firmware, as opposed to software) may be included, although not all of these may be available from a single vendor. Given the time, of course, a general purpose computer will perform all of these tasks, and more, but in photogrammetric control of dynamic processes the issue is speed with precision. Going through Table 1, all of the image processors perform single point arithmetic operations in real time (at the video rate). Those performing fast for the remaining operations in Table 1 belong to an exclusive, but growing, few. Some typical benchmark rates are: 30 ms. for 3×3 convolution filtering of a 500×500 pixel image, 60 ms. to derive a histogram of a 500×500 pixel image, geometric transformations in 30 ms. and a 1024 point Fourier Transform in 1 ms.

Today's hardware choice, exemplified by Fig. 3, is wide. Fig. 3a is a general purpose image processing system with micro VAX II class host and a full set of peripherals. Such systems may have optional coprocessors and are used most often in central processing, rather than for consideration in dedicated close range

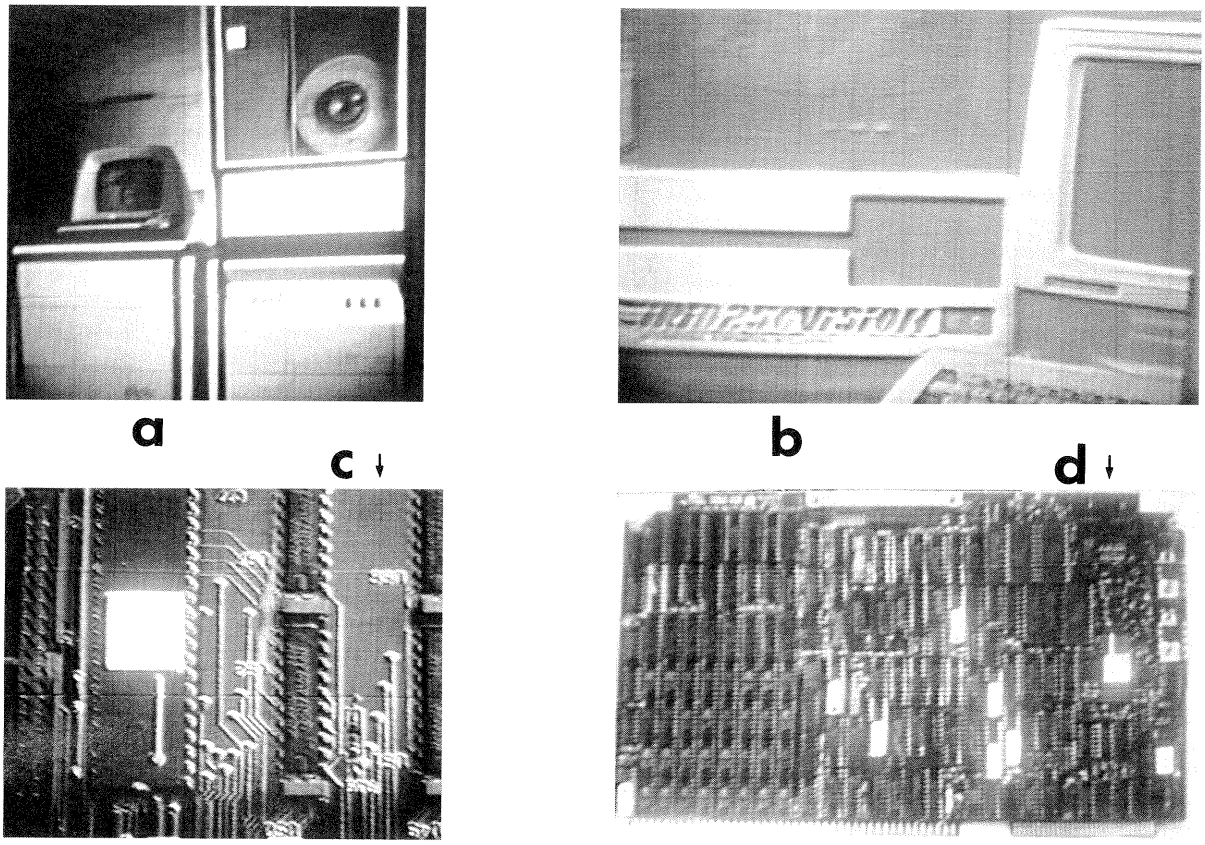

Fig. 3 (a) General purpose image processing system with peripherals.
(b) Compact, real-time image processing system.
(c) Single-chip digital signal processor.
(d) Board level image acquisition and processing module.

photogrammetric tasks, because of their relatively high capital cost and perhaps slower, generalized software.

Complete compact, stand alone, cost effective, real-time systems for dedicated applications are available, Fig. 3b. Image acquisition, including cameras, host computer, coprocessors, disc storage and software capable of supporting developments in real-time photogrammetry are a reality (at a $30,000 U.S. base level), El-Hakim, 1986.

The first single chip general purpose digital signal processor to have wide distribution was the TMS 32010 (1982 - Texas Instruments), McDonough, 1982, (the large integrated circuit in Fig. 3c). It is capable of real-time digital audio filtering but is too slow for real-time image operations, although it forms the basis for an image coprocessor for the IBM-PC, Pawle, 1984. It was an immediate commercial success because of the needs it filled at low cost and because of the unusual support from the manufacturer. In 1985 it captured 60% of the world single chip digital signal processor market as a result of a dramatic lowering of price from $750 at its introduction to $10-$15 in quantity today, demonstrating, once again, the remarkable anti-inflationary trend of modern electronics. A growing number of powerful single chip processors with potential future image application, Marrin, 1986, which may also be paralleled, are appearing, including the most recent 320 version, the TMS320C25.

Board level image processing products, Fig. 3d, represent an important category for close-range photogrammetric applications as well as the "small" system, Fig. 3b. They are most useful in well defined applications where photogrammetric software developed

elsewhere can be embedded into the system as firmware in electrically erasable read only memories (E^2PROM's). They are also valuable for the "open architecture" they represent, where new functionality is added with ease as it is developed. The first series of cost effective real-time board level imaging products with open architecture appeared in 1982, Hall, 1982. Choice was limited until mid 1985 when most of the functions in Table 1 became available in a series of modules, Siegal, 1985. Such modular systems are usually orchestrated by a small "host" computer given a modest level of software support by the vendor. (A personal computer may also be adapted to serve the purpose.) Communication is typically via two buses; the standard VME bus for general control and interfacing and a specialized high speed interboard video bus for digitized video, addressing and signal communication between modules. The arithmetic devices used in real-time systems are usually high speed multiplier accumulators. These have progressed from their introduction in 1978 as 8-bit word scalar devices to 32 bit word floating-point capability at 20 million multiply-accumulate operations per second today, Winard, 1986.

Photogrammetrists specializing in close-range real-time measurement and control of dynamic processes, particularly in engineering and manufacturing applications, may well consider investing in a dedicated system such as Fig. 3b for algorithm testing and software development, then, in cooperation with appropriate image processing module suppliers, specify applied systems using only the modules required. Time critical software can be imbeded as firmware in read only memories within the system. Computer integrated manufacturing solutions are particularly cost sensitive, demanding from the photogrammetrist his utmost skill for what undoubtedly will prove to be an endless range of highly different problems in 3-D measurement and control awaiting optimum solutions. Existing processing bottlenecks will dissolve as new, largely experimental, architectures evolve, Corbett, 1985, Lerner, 1985. A merging of electronics and optics in new multilevel logic devices also stands out as a radical departure opening unforeseen possibilities, Brody, 1986. Cost effectiveness, rather than elaborate technological solutions, will remain the key to manufacturing applications. Whatever trick works: sparse techniques, structured light, laser ranging, fiducial facets added to parts, etc., should be employed.

4. EQUIPMENT AND EXPERIENCE

The Photogrammetric Research Section at NRC has an example of each of the types of image processors shown in Fig. 3, El-Hakim, 1986. An upgraded Aries II Dipix system is utilized as a general purpose tool to explore different facets of photogrammetric image processing of pre digitized large format images and, in particular, for exploring error sources in digitized images, Havelock, 1984. An IRI Vision 256 system, Fig. 3b, is being used to explore a range of problems associated with real-time measurement and control of dynamic operations and for other applications such as automatic camera calibration, El-Hakim, 1986a. A TMS 32010 single chip digital signal processor, Fig. 3c, is part of an early evaluation module upon which some exploratory work was conducted to evaluate the potential of such processors in low end image processing, Real, 1985. This work ceased, becoming redundant by the very success of this chip which has found its way into over 2000 products.

The main thrust of the author's work has been the evolution of a board level system of open architecture for two quite different applications; a real-time, close-range medical application, Real, 1984, and one in visual communications for video based photogrammetric instrumentation, Real, 1985. Both of these applications had special requirements not met by commercial products, but future need for in-house development of this nature should be minimal. Special considerations for a system in which the most important function for the image processor is transformation of a moving stereo image for a human operator is outlined elsewhere, Real, 1986. Some results from the author's system developed (and still evolving) in-house are included to illustrate the potential of multiprocessing modules, (see also Real, 1986). It must be noted that relevant detail may become lost in the reproduction and that the actual images are displayed on a color monitor with graphics in a contrasting color that does not show well in some of the black and white reproductions.

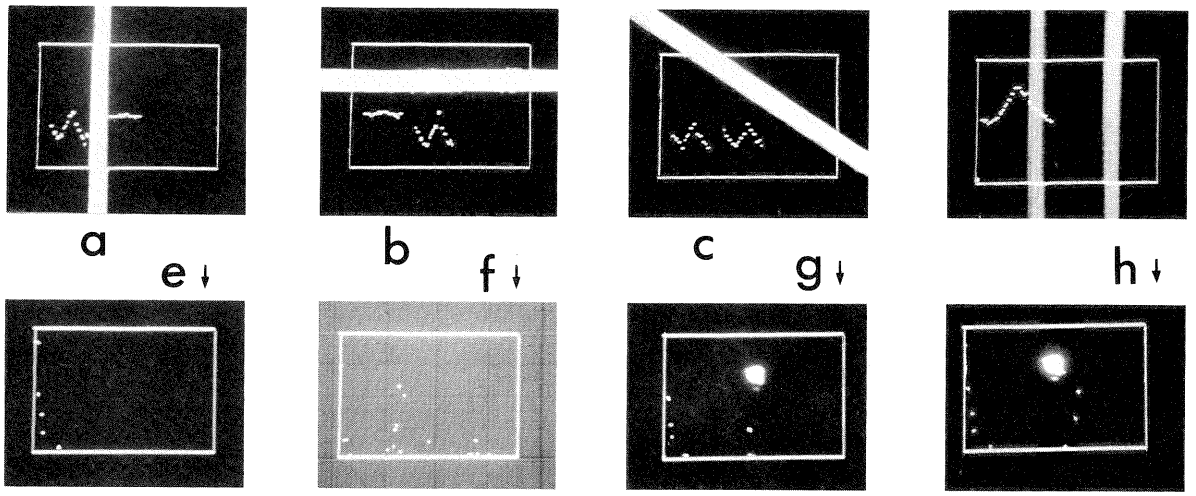

Fig. 4

(a),(b),(c) x,y image autocorrelation.
(d) Image convolution in x.
(e)-(h) Image histogram peaks:
(e) dark field.
(f) moderately uniform field of medium intensity.
(g) bright spot in dark field.
(h) higher intensity version of (g).

An autocorrelation function is shown in Figs. 4a, b, c. Fig. 4d is an x axis convolution of the image, useful for detecting left-right symmetry, Real, 1984. That symmetry exists is indicated by a singular cusp, Fig. 4d, while the position of the pattern with respect to frame center is disclosed by the lateral shift of the cusp. Note that such graphic displays aid in observing events and trends, but that the digital results from which these are derived are normally used directly in the digital domain for automatic decision, measurement and control systems.

Image histogram capture and display is illustrated in Figs. 4e-h. The ordinate represents the relative frequency of occurrence of an image intensity level and the abscissa the relative intensity (dark to the left, bright to the right). Fig. 4e is indicative of a "dark field", 4f a fairly uniform "medium bright field", 4g an illuminated region in a dark field and 4h the same as 4g with higher intensity. The values have been biased to show only the relevant peaks. (In case the reproduction is not clear, Fig. 4e has a peak near abscissa zero, 4f approximately one-third from the left, 4g near zero and at a point below the bright spot, Fig. 4h near zero and just to the right of the bright spot.) Histogram acquisition occurs in parallel with image transformation and correlation operations. The data is used to precondition an image prior to other operations or as a measuring tool for transformation or image identification. The data can be used to specify a new histogram, Biegel, 1985; but histogram specification assumes operator feedback and is not easy to implement in an automatic system. Histogram equalization, Scher, 1980, can be implemented rapidly by using the histogram result to choose the closest of one of a number of prestored look-up tables to approximate the desired equalization.

The effect of image processing upon light intensity distribution is illustrated in Fig. 5. Fig. 5a shows an "original" image with histogram having broad responses at low, medium and higher light intensities. After contrast reversal and compression, most of the energy is seen to fall in a narrow range indicated by the single cusp nature of the histogram in Fig. 5b. These histograms, biased to show only significant

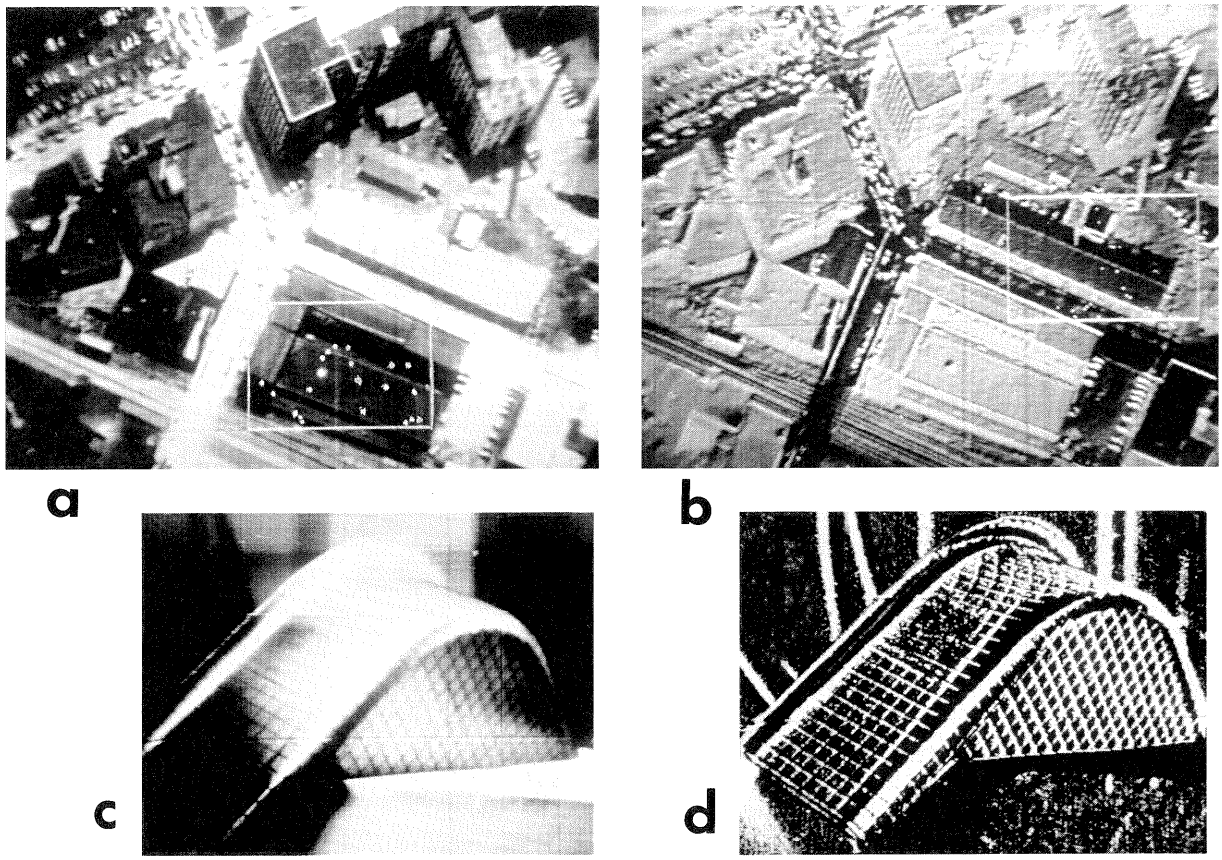

Fig. 5
(a) Image with histogram.
(b) Processed image with histogram

3×3 kernel

$$\begin{vmatrix} -12 & -12 & -8 \\ 12 & 0 & -12 \\ -12 & -14 & 12 \end{vmatrix}$$

(c) Metal part with printed grid.
(d) Image (c) processed with kernel

$$\begin{vmatrix} 13 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -15 \end{vmatrix}$$

peaks, are formed in 17 ms. from alternate pixels in one video field. Of more interest for industrial measurement is image transformation (by convolution filtering) to precondition an image prior to analysis, Figs. 5c and d. The grid painted onto a metal part reflecting highly varying amounts of light back to the camera is rendered almost entirely visible and binary in appearance.

Finally, Fig. 6a shows part of an aerial photograph with the windowed region autocorrelated along the major window x, y axes. Fig. 6b shows the same photograph with the smoothing convolution filter applied, indicated by the broader x, y autocorrelation and in Fig. 6c a high pass filtering with narrowed autocorrelations (may be rather obscured in the reproduction). These are a few examples of real-time image processing operations attainable with relatively low cost modules and applicable to real-time, close-range photogrammetric problems.

7. CONCLUSION

Measurement and control of dynamic 3-D processes is at the heart of computer integrated manufacturing. A wide assortment of ad hoc approaches has been used to simplify and solve the many and varied problems. Today's and tomorrow's image

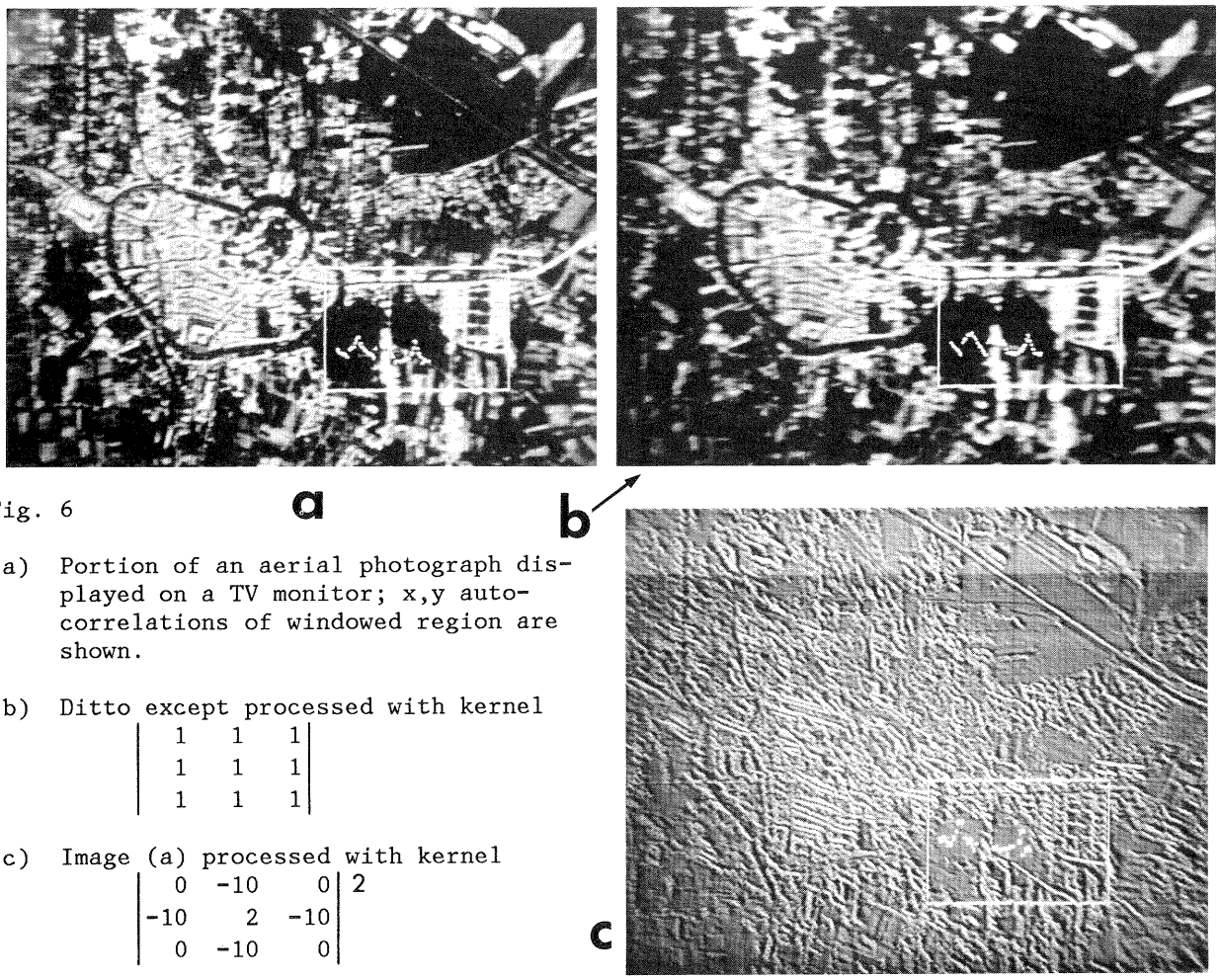

Fig. 6

(a) Portion of an aerial photograph displayed on a TV monitor; x,y autocorrelations of windowed region are shown.

(b) Ditto except processed with kernel

$$\begin{vmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{vmatrix}$$

(c) Image (a) processed with kernel

$$\begin{vmatrix} 0 & -10 & 0 \\ -10 & 2 & -10 \\ 0 & -10 & 0 \end{vmatrix} 2$$

acquisition and processing hardware allows the photogrammetrist to develop novel 3-D measurement algorithms that solve the problems and lend these systems a degree of intelligence and precision heretofore unattainable. This paper has attempted to convey to the photogrammetrist where the electronic technology is at a time when "superchips", like the 2048×2048 pixel imager, the 4 Mbit memory and the mainframe computer on a chip, are becoming fact from fiction.

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