

# The Development of a PC-based Near-Real-Time Photogrammetry System PHOENICS

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## **Abstract**

The first development stages of a low cost PC-based Near Real-Time Photogrammetry system PHOENICS are discussed. Hardware and software components are described and planned system enhancement stages are sketched out. Concepts employed for target detection and analysis are briefly discussed. A target centre detection technique in which a combination of original and thresholded image is employed and a target design especially suited for thresholding techniques is presented. The introduction of parallel processing hardware into PHOENICS as a next enhancement phase is suggested. Accuracies achieved in first experiments with the prototype of PHOENICS are reported.

## **1. Introduction**

Photogrammetrists worldwide have responded to the challenge presented by the developments in computer hardware, solid state cameras and image processing technology. A number of so-called Real-Time Photogrammetry (RTP) or Near Real-Time Photogrammetry ( NRTP) camera systems have emerged in recent years and successful applications to close range photogrammetry problems have been reported (Kratky 1979 , El-Hakim 1986, Haggrén 1986 , Grün 1987a,1987b, Wong 1986 ). Most of these systems rely on expensive hardware components with mini computers or even main frame type computers as host. Reduced prices and increased capabilities in Personal Computer technology have brought NRTP, if not RTP, within range of a much broader group of photogrammetrists and PC-RTP research is likely to experience a period of considerable advancements.

This paper describes the first successful stages of the design of PHOENICS (**Photogrammetric engineering and industrial digital camera system**), which is an example of such a low cost PC-based NRTP system. The development of PHOENICS is clearly an ongoing project and, besides the description of hard and software components, special emphasis is placed on the discussion of system enhancements. Although PHOENICS is operational, it is only a prototype and room for improvement appears limitless. Especially the area of parallel processing technology offers possibilities which will bring PC- systems closer to true 'Real Time Photogrammetry'.

## 2. System hardware

**PHOENICS** is designed as a low cost system and consequently a number of compromises have had to be made in the choice of the hardware components. In all cases attempts were made to satisfy minimum requirements without significant loss of quality. In the original hardware configuration speed and system capacity are restricted. Also, the present limitation to two cameras confines somewhat the application areas of the initial system. However, as discussed later, the configuration described here is merely for prototyping and initial software development with the aim to eventually develop and optimise hardware and software towards a 'Nearer to Real-Time' system.

### 2.1 Hardware configuration

The present hardware configuration of PHOENICS (Fig. 1) comprises :

- a Personal Computer - IBM Personal System /2 Model 30
- a Video Frame Grabber - Matrox PIP-512 board
- two CCD cameras - Siemens K211
- two external monitors - Phillips RGB monitors CM 8833

It is intended soon to enhance this prototype version of PHOENICS by a larger frame grabber board and the acquisition of parallel processing hardware and further cameras for all round imaging.

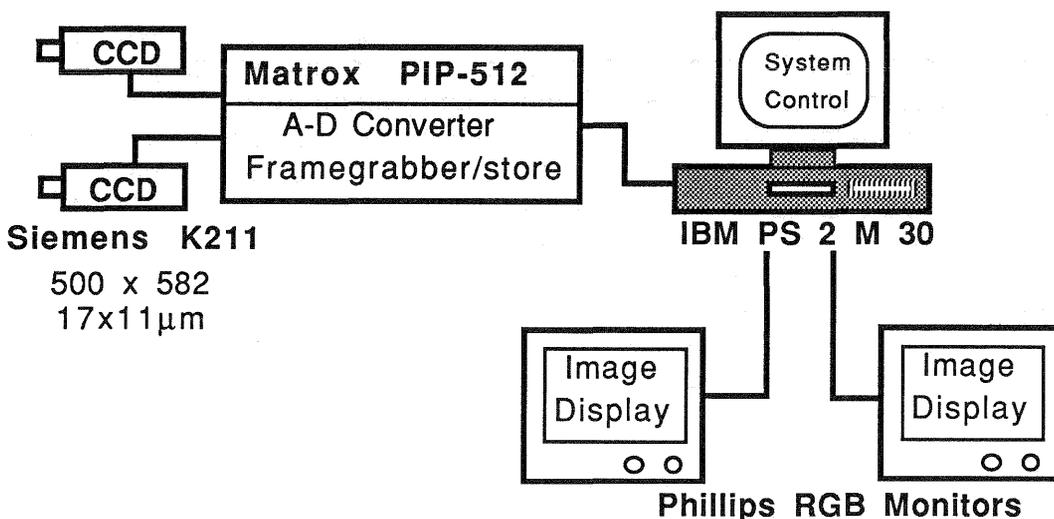


Fig. 1 PHOENICS Hardware configuration.

## 2.2 The Host Computer

The criteria for the choice of the computer were

- low cost, off-the-shelf hardware components
- high resolution graphics with a large range of grey shades for the display of images on the computer screen
- compatibility with low cost, high performance floating point hardware (Intel 8087 co-processor)
- compatibility with parallel processing hardware
- availability of specialised hardware for the system (frame grabber boards and parallel processors )
- system portability

The IBM-Personal System/2 Model 30 with a high resolution monochrome screen satisfied these conditions. A VGA-high-resolution graphics card provides formats of 640 by 400 with 16 shades of grey and 320 by 200 with 64 shades of grey . At the present stage of the development of PHOENICS a choice is given between a reduced image (every other pixel is displayed) on the PC screen or complete images on the two external RGB monitors.

Model 30 is equipped with an Intel 8086 microprocessor running at 8 MHz, a 16-bit internal bus and a 8087 Co-processor. It is the only model in the PS/2 range which will accept standard PC-cards.

## 2.3 The cameras

The system's cameras are two monochrome solid state CCD cameras (Siemens K211, SONY XC-57 CE CCD chip) with the European CCIR video standard of 625 lines at 50 Hz . This provides a frame rate of 25 Hz. The CCD image sensor is of the interline transfer type and has dimensions of 8.8 (horizontal) by 6.6 (vertical) mm which is equivalent to a 2/3" imaging tube. The cameras are equipped with a 17 mm and a 12.5 to 75 mm Zoom lens. The sensor's resolution is 500 by 582 pixels with a physical pixel size of 17 by 11  $\mu\text{m}$ . However, only 468 by 568 pixels of this array are active in the imaging process and the active chip area is only 8.4 by 6.4 mm. Similar reductions in imaging area must be expected for most CCDs, although they are usually not reflected in the technical information supplied with the camera.

CCD cameras are, due to their fixed pixel arrays, more suited to metric image analysis than conventional Vidicon cameras. The collective term 'digital' camera which is generally used for CCD and CID cameras may be somewhat misleading and should, strictly, only be used for cameras with digital output. The majority of the pixel array cameras (Grün, 1987) do not provide a digital output of a grey value for each pixel . Instead the camera's output is a continuous analogue amplitude modulated signal, which requires conversion into digital form by means of an A/D converter. However, there is some justification for including CCD and CID cameras with analogue output into the family of digital cameras as it is possible to obtain the position of each pixel within the array in digital form.

## 2.4 The Video Digitiser

The A/D converters of most framegrabbers resolve the analogue light intensity signal coming from the camera into 8 bit pixels which is equivalent to 255 shades of grey, ranging from 0 for black to 255 for white or vice versa. At a frame rate of 25 frames per second it becomes necessary to cope with data sets of 0.25 million 8-bit bytes in 1/25 second.

The operations typically executed on the camera/framegrabber combination for each image are, in simplified form :

1. Image integration and transfer on CCD sensor
2. Output of image in analogue form
3. Digitising of the video image, that is converting the analogue signal into 8-bit bytes by means of an A/D converter
4. Passing the data through a LUT (Look Up Table) in which the grey values coming from the camera are transformed for output in a user-selected form (for example transformed from positive to negative image, contrast enhanced or thresholded)
5. Storing of the image in the board buffer
6. Converting the image from digital to analogue (D/A converter) for display on a monitor (this step is not essential as the image does not necessarily need to be displayed).

Steps one and two are camera functions, the remaining steps must be executed by an external processor.

No conventional PC can cope with these demands within 1/25 second and it is necessary to introduce additional processing power into the PC. This can be done by installing a video digitiser board, also known as frame grabber/frame store or, if image processing software is included, as IP board. The frame grabber boards are dedicated to A/D conversion, frame grabbing and frame store.

A number of these boards with varying degree of performance and sophistication are commercially available. It also appears, that frame grabbers have captured the imagination of the electronic DIY world and in recent months circuit diagrams with building instructions for such boards have found their way into technical and DIY journals. Building a tailor made board for a photogrammetric camera system has the advantage that the framegrabber parameters can be chosen to suit the CCD array of the system camera without the loss of any part of the image. (A 'home made' board for PHOENICS is under construction.)

The commercially produced image processing boards are generally supported by software libraries with an often surprising range of imaging, image enhancement and image processing routines.

Boards and software are designed with image processing application in mind but can be readily adapted for photogrammetric camera systems. This is possible as most boards allow the addition of own software into the IP libraries or the use of the IP commands in one or more of the widely used PC languages such as FORTRAN, C or PASCAL. Most boards are designed to fit directly into IBM PC, AT and compatibles.

For PHOENICS a MATROX PIP-512 board was chosen. A second, larger board, PIP-1024, has since been added to the PC to allow simultaneous stereo imaging from two cameras for dynamic processes. The board, like all other commercially available frame grabbers, is not specifically designed for metric analysis of the image. Its main capabilities lie in the area of capturing and processing of images for qualitative information extraction. The bulk of the software included with the board is often of little or no use to a photogrammetric camera system. In this context only those properties of the boards which are relevant to photogrammetric application are of importance.

The PIP - 512 board digitises the analogue signal from the camera into 512 by 512 8-bit pixel values. Unless a frame grabber is designed for a specific CCD or CID camera, the A/D conversion of the analogue signal coming from the camera produces pixels which are neither in size nor configuration identical to the original camera pixels. In the case of the Siemens/MATROX camera/video board combination the original active camera pixel array of 468 by 568 is converted to a 512 by 512 field, the camera pixel of 17 by 11  $\mu\text{m}$  is transformed into a 15 by 11  $\mu\text{m}$  pixel equivalent by the PIP board. Some 15 % of the camera image is lost.

The change in the pixel size can be allowed for in form of affine scalefactors. The scalefactors can either be treated as unknowns in the least squares model of the conventional photogrammetric solution or predetermined in a calibration process. The fact that part of the image is lost in the digitising process is obviously a disadvantage. However, this shortcoming can be allowed for by an appropriate camera object configuration.

The board can store a 256 Kbyte image on its on-board-buffer. It allows three cameras to be connected simultaneously but the images can only be taken sequentially and require an empty buffer for each new image. This means that the buffer content must be transferred to the host's RAM before the next image can be captured resulting in delays between consecutive images. In practical applications the delay between images is only relevant if dynamic processes are monitored or if the object is unstable.

Additional boards allow truly simultaneous capture of images. The system can support four boards with three channels each so that up to twelve cameras could be connected to the system, four of these cameras can be activated simultaneously.

Three approaches to image storage can be adopted :

- 1- original images are fully stored
- 2- enhanced images are fully stored
- 3- relevant information (e.g.image coordinates of points) is extracted before storage and only this information is stored

If full images are stored then the time required to move the image out of the boards buffer to some other storage device controls the time between images. It could be compared to advancing the film in conventional photography .

The PIP board allows the following transfer/storage facilities for the image :

- 1- the image can be held in the video buffer of the board  
( this option is only viable if a single image is taken).
- 2- it can be transferred to system memory using DMA
- 3- it can be transferred to system memory using a RAM (virtual) disk
- 4- it can be transferred to the system's hard or floppy disk

Times required for capturing and storing a single image differ between 0.04 sec and 4 seconds depending on the storage method used.

PHOENICS presently gives a choice between immediate target extraction with storage of target centres only and full image storage on disk with subsequent target extractions. Immediate target extraction is faster but has the obvious disadvantage that the image itself is lost. The decision as to which method is preferable depends on the application case.

## **2.5 Parallel Processing software**

The next stage planned for the PHOENICS development is the incorporation of parallel processing hardware into the system in order to increase raw processing power and move further into the direction of Real-Time Photogrammetry.

There are currently two types of parallel processing hardware available for use in IBM PC, AT and compatible.

1. INMOS Transputer based cards from Definicion Systems, Microway and other manufacturers.
  - raw processing power about 7 MIPS (T414)
  - programmable in C
  - code for use in nodes CANNOT be tested and debugged on the host (IBM or compatible systems)
2. INTEL 8088 compatible based card from Human Devices.
  - raw processing power about 1 MIP (10 MHz NEC V20 CPU)
  - programmable in C
  - code for use in nodes CAN be tested and debugged on the host.

The 8088 compatible based nodes provide parallel processing at lower cost and allow faster development of node software as the software may be debugged in the host system. These factors make 8088 compatible based nodes attractive for system development and prototyping. Since software for both node types is written in C it can be transported (with the exception of communication enhancements) between the two types of nodes.

## 2.6 Parallel processing in the PHOENICS system configuration

The Intel 8086 CPU of the PS 2/ Model 30 is the least powerful processor in the PHOENICS configuration and as such is best used for those tasks which require the least processing power. After installation of the parallel processor card into PHOENICS the system will therefore be configured for the 8086 to function as the systems control processor, I/O processor and dispatcher.

As a Control Processor the 8086 will be responsible for

- controlling the overall flow of the software
- controlling the image processing board

as an I/O processor for

- controlling the transfer of image data from the image processing hardware to the PC using DMA (Direct Memory Access)
- passing data to the transputer over the transputer link

and as a dispatcher for

- optimal utilisation of available transputers
- initiating and synchronising the parallel processors

The 8086 will also function as a processor

- for software portions not suited to parallel processing

The size of the transputer network which can be supported by the software and hardware is limited only by the number of expansion slots (in the system unit and expansion chassis) and by power supply capacity.

In PHOENICS the parallel processors will be responsible for the processing-intensive stages of the RTP process and software is designed to invoke parallel processing at the earliest opportunity. Distributing sections of the image to the available processors might be an obvious way to utilise parallel processing but it is not always practical. PHOENICS software produced uses a simple and fast target detection algorithm followed by a more sophisticated target analysis. This concept makes it possible to pass individual target analysis to the available parallel processors once a point has been detected while target search on the remaining image continues on the host system.

It is planned to later enhance the system further by using "rule based" Artificial Intelligence (AI) languages such as Lisp or Prolog for target analysis and image matching. AI languages are processing-intensive and parallel processors have the processing power to support these languages.

### **3. Choice of programming language and compiler**

It was decided to use C as the programming language of PHOENICS.

- C - is portable
- allows production of compact fast executing code
- allows control of and communication with parallel processors
- is frequently used to control image processing hardware.

Of the available C compilers Microsoft C was chosen as it may be used with the support software and the libraries supplied with the PIP-512 software and parallel processing hardware.

## **4 System Software**

The system software combines own software with image capturing and processing routines provided with the PIP 512 card. At the present stage of development images can be captured, stored in various forms, enhanced and thresholded. Noise can be reduced, targets can be detected and target centers can be found without operator assistance. Target coordinates are provided and targets are indicated by circles displayed on the RGB monitors.

Independent image correlation does not yet form part of PHOENICS. Instead the operator is prompted by the software to identify points indicated on the RGB monitors. In the final phase (the photogrammetric treatment of the images) projective transformation is used to determine object point coordinates. Development of image correlation algorithms and selfcalibration bundle adjustment in C are in progress.

### **4.1 Image Simulation**

During the ongoing development phase of PHOENICS need has arisen for an ideal digital image with controllable parameters. This was achieved by image simulation and a program for the creation of simulated 'best case' images was written for the testing of concepts, algorithms and debugging of code.

The program allows the user to introduce targets of various types in positions controlled by user defined camera-object configurations. These positions are easily evaluated using the well-established perspective relationships known from conventional photogrammetry.

Parameters controlling the digital properties of the image allow the user to choose

- pixel array format and range of grey scale
- grey value of background
- introduction of random noise
  - percentage of noise in overall image
  - range of grey values of noise
- target size and type from a set of predesigned targets (circle, ellipses, cross)

For the design of the simulated targets a model was adopted in which pixels covered fully by the point-image are given a grey value corresponding to black. Unaffected pixels have the same value as chosen for the image background. Partially covered pixels are allocated intermediate values proportional to the portion of the pixel covered.

Target arrays are designed in a manual-graphic process in which the desired target is drawn at a large scale onto a grid, where each grid square represents one pixel. Covered areas of partially affected 'pixels' are measured on a digitiser board. Figure 2 shows the example of a simulated ten by ten pixel array representing a circle with radius 9 and a centre position of 5.3 (hor.) and 5.4 (vert. pixel count). For the example the background is assumed to have a grey scale of 0, no noise is overlaid.

#### 4.2 Target, target detection and analysis

For the detection of the target, image thresholding followed by automatic target detection appears to be the most widely used technique (Grün 1986, Haggren 1984, Wong 1986) in Real-Time photogrammetry.

	1	2	3	4	5	6	7	8	9	10
1	0	0	0	0	22	45	9	0	0	0
2	0	0	60	205	255	255	251	153	13	0
3	0	49	242	255	255	255	255	255	190	4
4	0	206	255	255	255	255	255	255	255	110
5	27	255	255	255	255	255	255	255	255	194
6	57	255	255	255	255	255	255	255	255	210
7	10	251	255	255	255	255	255	255	255	180
8	0	169	255	255	255	255	255	255	255	79
9	0	19	212	255	255	255	255	255	153	0
10	0	0	12	133	214	236	180	84	0	0

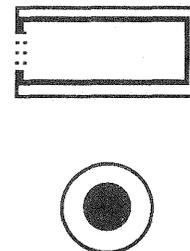


Fig.2 Simulated pixel representation of a circular target (r=9 centre 5.3 h 5.4 v) with a background grey value 0.

Fig.3 'Black hole' target Cross section and front view.

Thresholding creates a binary image in which all pixels below a chosen threshold-grey value are given value 0 and all remaining pixels value 1 (or some other value pair). This technique relies on a significant difference between the light emission from object and target - targets must either be considerably darker or brighter than any other part of the image. Thresholding/target detection algorithms are adversely affected by the possible presence of noise of a grey level similar to that of the target.

In most cases 'noisy' pixels or pixel groups can be removed by standard routines supplied with image processing libraries. In addition to this, size and form of detected pixel groups can serve as criteria for rejection or acceptance as targets.

PHOENICS thresholds the image followed by noise removal, scanning for targets and an approximate point centre determination. Information is lost in the thresholding and noise removal algorithms and pixel values are changed. The final target-centre determination is therefore executed on the original image. A suitably sized mask is placed over the individual targets on the basis of target position as extracted from the thresholded image. Point positions shift typically by up to 0.5 pixels when found on the original image instead of the thresholded image.

Target centres are determined as arithmetical pixel mean on the thresholded image and by moment reduction or weighted mean (Wong 1986) on the original.

## **5. Target design**

The design of targets for control and object points must be guided by the target detection algorithm of the RTP system. Original attempts to design targets for thresholding with PHOENICS were less successful. Active light emitting targets were rejected as impractical for many applications, while passive light emission targets are still under investigation. The other end of the grey scale, a black target type, was then investigated. No material or paint could be found which was light absorbing enough to provide a contrast with most other surfaces sufficient to allow reliable thresholding. Most targets tested showed spurious reflections from parts of the target surface.

The answer was found in a 'black hole' target design (Fig. 3). A hollow cylinder, closed on one side was covered by a thin disk with a central, circular hole on the other. The inside was painted with a black paint of minimum reflectance and the outside white. The thus created hole is non-reflecting and provides a practically ideal control point target for thresholding methods. The disadvantage of the design is that, as is the case with light emitting targets, it can not always be easily attached to relevant object points.

## **6. First results and accuracies.**

First experimental measurements proved most encouraging. A control field of targeted points distributed over a range of approximately 0.6 x 0.6 x 0.6 m was coordinated in XYZ using a UMK-10 camera. The field was then imaged using the PHOENICS cameras at a distance of 1.7 m from the base. Point thresholding, detection and centre determination was executed without operator assistance, while point identification was done by inspection followed by a projective transformation

adjustment. Five images were taken from each camera position in quick succession and the results were averaged. Average standard deviations of repeated point centre determinations were 0.08 pixels (or 1  $\mu\text{m}$ ) with maximum differences between determinations of the same point centre of 0.5 pixels (or 7  $\mu\text{m}$ ). Object point positions deviated from those obtained with the UMK cameras by an average of 0.5 mm in x and y and 1.1 mm in z. Standard deviations were  $\sigma_{x,y} = \pm 0.4$  mm and  $\sigma_z = \pm 0.8$  mm.

When judging these accuracies it must be realised that the projective transformation software used does not allow for the introduction of a controlled model for chip or lens distortions. Accuracy improvements are expected once software for a selfcalibration bundle adjustment with additional parameters is completed and incorporated into PHOENICS.

## 7. Conclusions

The first phase of the development of the low cost PC based NRTP system PHOENICS has been successfully completed. The system is operational and positions of targeted points have been determined with accuracies of 0.5 to 1 mm over a distance of 1.7 m from the camera base. Operator assistance is minimal and restricted to the identification of points by inspection after the point positions have been found unassisted.

The two-step-determination of targets, first on a thresholded and then on the original image, has shown to be an efficient and accurate way of determining point centre positions. The 'black-body' target design appears to be ideally suited to thresholding methods.

PC hardware can play a significant role in the development of Real-Time Photogrammetry systems. However, to approach true RTP the introduction of parallel processing hardware into RTP systems would appear to be the direction in which research must proceed. Interest should be centred on software which optimises:

- management of images within the hardware configuration
- task allocation to parallel processors
- image analysis algorithms
- image correlation algorithms
- algorithms related to the photogrammetric model

The optimisation criteria should be speed and accuracy with priorities being determined by specific applications. In PHOENICS a modular software concept is aimed for in which a general RTP system can be optimised for a specific application by the choice of a suitable module combinations.

Development phases for PHOENICS incorporating parallel processors and automatic image correlation respectively as well as improved photogrammetric software have been initiated.

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